MITSUBISHI ELECTRIC

<DIPIPM >

Large DIPIPM+ Series APPLICATION NOTE

PSSxxNE1CT

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Large DIPIPM+ Series Application note

CHAPTER 1 : INTRODUCTION

1.1 Feature of Large DIPIPM+

Large DIPIPM+ series is our latest transfer molding CI type IPM(CI: Converter Inverter, IPM: Intelligent Power Module). It integrates the inverter and converter parts to make up a compact inverter systems for commercial and industrial inverter application like commercial air conditioner, servo and general purpose inverter.

General DIPIPM integrates a inverter part only, but recent market demand requires highly integrated IPM products including more functions and peripheral circuits. So we have realized the All-in-One DIPIPM, “DIPIPM+”. DIPIPM+ series is well designed transfer molding package from our long term history as the pioneer. New Large DIPIPM+ series is expanded power capacity.

Large DIPIPM+ integrates main components for inverter circuit and it will contribute to reduce total cost by smaller mounting area for inverter circuit, shorter designing time and more reasonable assembly cost. It employs similar general DIPIPM series function. So Large DIPIPM+ series enable same system design for its inverter part like general DIPIPM series.

By adopting same structure of heat radiation as Large DIPIPM series which has high thermal conductivity, it is possible to design system with high reliability.

Main features of this series are described as follows;

- ***Newly optimized CSTBT are integrated for improving performance***
- ***1200V series covers from 35A to 100A rating lineup***
- ***Easy to design a PCB pattern wiring by smart terminal layout***
- ***Easy to use temperature output function of the sensor integrated on control IC***

Fig.1-1 shows package photograph and Fig.1-2 shows the cross-sectional structure.

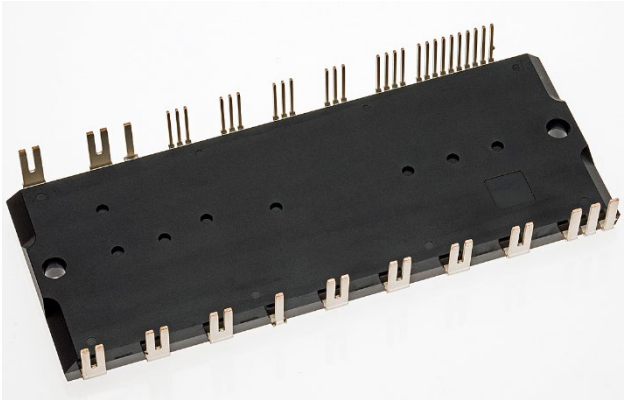


Fig.1-1. Package photograph

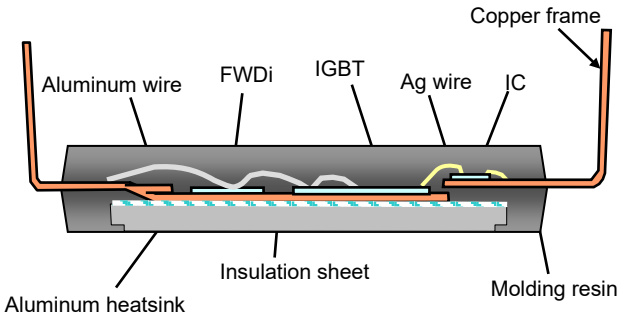


Fig.1-2 Cross-sectional structure

1.2 Functions

Inverter block

●For P-side IGBT
- Drive circuit
- High voltage level shift circuit
- Control supply under voltage (UV) lockout circuit (without fault signal output)

●For N-side IGBTs:
- Drive circuit;
- Short circuit (SC) protection circuit (By detecting sense current divided at N-side IGBT with external sense resistor)
- Control supply under voltage (UV) lockout circuit (with fault signal output)
- Outputting LVIC temperature by analog signal (No self over temperature protection)

●Fault signal output
- Corresponding to N-side IGBT SC protection and N-side UV protection.

Common items

●IGBT drive supply
- Single DC15V power supply

●Control input supply
- High active logic with 5V

●UL recognized
- UL1557 File E323585

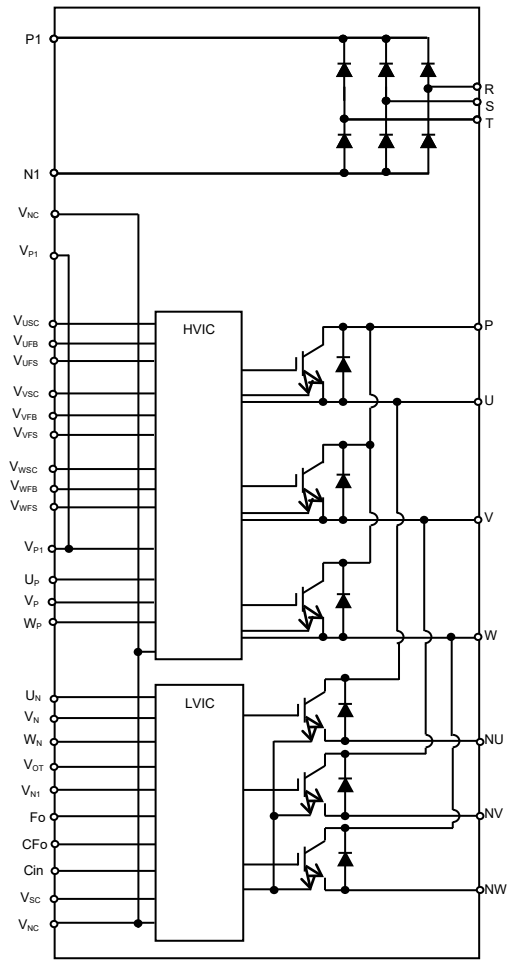


Fig. 1-3 Internal circuit block diagram

1.3 Applications

Motor drives for low power industrial equipment and commercial equipment such as air conditioners

1.4 Line-up

Line-up is described as following table 1-1.

Table 1-1. Large DIPIPM+ line-up

Type name	Rated current	Rated voltage	Motor ratings (note1)	Isolation voltage
PSS35NE1CT	35A	1200V	5.5kW/440V_{AC}	2500Vrms(note2)
PSS50NE1CT	50A		7.5kW/440V_{AC}	
PSS75NE1CT	75A		11kW/440V_{AC}	
PSS100NE1CT	100A		15kW/440V_{AC}	

(note 1)
The motor ratings are described for industrial and general motor capability, and actual ratings are different with application condition.

(note 2)
Isolation voltage is tested under the condition of which all terminals are connected with conductive material and DIPIPM+ is applied 60Hz sinusoidal voltage between the terminals and heatsink for 1minute.

1.5 The Differences of Previous Series (DIPIPM+ and Large DIPIPM Ver.6) and This Series

There are some differences between this Large DIPIPM+ series and DIPIPM+ (PSSxxMC1FT/PSSxxNC1FT) and Large DIPIPM Ver.6 series (PSSxxSA2FT) as below Table 1-2.

Table 1-2 Differences of specifications

Item	Large DIPIPM Ver.6	DIPIPM+	Large DIPIPM+	Ref.
	PSSxxSA2FT	PSSxxMC1FT, PSSxxNC1FT	PSSxxNE1CT	
	5A～75A	5～35A	35~100A	
Built-in IGBT	6th IGBT(1) (LPT-CSTBT)	6th IGBT (LPT-CSTBT)	7th IGBT (LPT-CSTBT)	-
Internal circuit	6in1	CIB or CI	CI	-
Bootstrap Di	Built-in (with current limit R typ. 20Ω)	←	Nothing	-
T_j	-30°C ~150°C	←	—	-
T_{jop}	—	←	-30°C~150°C	
T_{jmax}	—	←	175°C	
Temperature output (V_{OT} Output)	typ. 2.38V (LVIC temp.=75°C) with pull down resistor	typ. 3.02V (LVIC temp.=100°C) with pull down resistor	←	Section2.2.3
SC protection	**Sense resistor** (By detecting sense current divided at N-side IGBT)	**Shunt resistor**	**Sense resistor** (By detecting sense current divided at N-side IGBT)	Section2.2.1
t_{dead}	min. 3.0μs	←	min. 2.5μs (35A/50A/75A) min. 3.0μs (100A)	-

(1) PSS75SA2FT(75A/1200V) is Only 7th IGBT(LPT-CSTBT)

There are other differences. (e.g. electric characteristics, sense resistance for SC protection, electrical potential of dummy terminals, thermal resistance and allowable minimum pulse width)
Please refer each datasheet for more detail.

CHAPTER 2 : SPECIFICATIONS and CHARACTERISTICS

2.1 Specification of Large DIPIPM+

It is representatively described as follows with PSS50NE1CT (50A/1200V).
For the other products, please refer each data sheets in details.

2.1.1 Maximum ratings

Maximum ratings are described as following table 2-1-1. (T_j = 25°C, unless otherwise noted)

Table 2-1-1 Maximum rating of PSS50NE1CT (50A/1200V)

MAXIMUM RATINGS (T_j = 25°C, unless otherwise noted)

INVERTER PART

Symbol	Parameter	Condition	Ratings	Unit	
V_{CC}	Supply voltage	Applied between P-NU,NV,NW	800	V	(1)
$V_{CC(surge)}$	Supply voltage (surge)	Applied between P-NU,NV,NW	1000	V	(2)
V_{CES}	Collector-emitter voltage		1200	V	(3)
$\pm I_C$	Each IGBT collector current	T_C= 25°C (Note 1)	50	A	(4)
$\pm I_{CP}$	Each IGBT collector current (peak)	T_C= 25°C, up to 1ms	75	A	
T_{jop}	Junction temperature	Continuous operation (Note 2)	-30~+150	°C	(5)
T_{jmax}	Maximum Junction temperature	Instantaneous event(overload)	175	°C	

Note1: Pulse width and period are limited due to junction temperature.
Note2: The maximum junction temperature rating of built-in power chips is 175°C(@Tc≤125°C).However, to ensure safe operation of DIPIPM, the average junction temperature should be limited to Tj(Ave)≤150°C (@Tc≤125°C).

CONVERTER PART

Symbol	Parameter	Condition	Ratings	Unit
V_{RRM}	Repetitive peak reverse voltage		1600	V
Io	DC output current	3-phase full wave rectification	50	A
I_{FSM}	Surge forward current	Peak value of half cycle at 60Hz, Non-repetitive	532	A
I^2t	I^2t capability	Value for 1 cycle of surge current	1132	A^2s
T_j	Junction temperature	(Note 3)	-30~+150	°C

Note3: The maximum junction temperature rating is 150°C. But for safe operation, it is recommended to limit the average junction temperature up to 125°C.

CONTROL (PROTECTION) PART

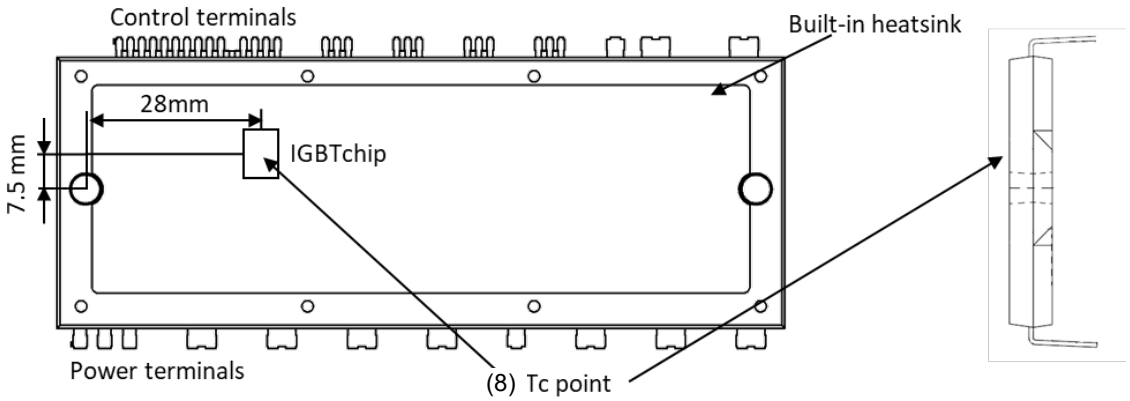
Symbol	Parameter	Condition	Ratings	Unit
V_D	Control supply voltage	Applied between V_{P1}-V_{NC}, V_{N1}-V_{NC}	20	V
V_{DB}	Control supply voltage	Applied between V_{UFB}-V_{UFS}, V_{VFB}-V_{VFS}, V_{WFB}-V_{WFS}	20	V
V_{IN}	Input voltage	Applied between U_P,V_P,W_P,U_N, V_N, W_N-V_{NC}	-0.5~V_D+0.5	V
V_{FO}	Fault output supply voltage	Applied between F_O-V_{NC}	-0.5~V_D+0.5	V
I_{FO}	Fault output current	Sink current at F_O terminal	5	mA
V_{SC}	Current sensing input voltage	Applied between CIN-V_{NC}	-0.5~V_D+0.5	V

TOTAL SYSTEM

Symbol	Parameter	Condition	Ratings	Unit	
$V_{CC(PROT)}$	Self protection supply voltage limit (Short circuit protection capability)	V_D = 13.5~16.5V, Inverter Part T_j = 150°C, non-repetitive, less than 2μs	800	V	(6)
T_C	Module case operation temperature	(Note 4)	-30~+125	°C	
T_{stg}	Storage temperature		-40~+125	°C	
V_{iso}	Isolation voltage	60Hz, Sinusoidal, AC 1min, between connected all pins and heat sink plate	2500	V_{rms}	(7)

Note4: Measurement point of Tc is described in below figure.

Large DIPIPM+ Series Application note



No.	Symbol	Description
(1)	V_{CC}	The maximum voltage can be biased between P-N. A voltage suppressing circuit such as a brake circuit is necessary if P-N voltage exceeds this value.
(2)	$V_{CC(surge)}$	The maximum P-N surge voltage in switching status. If P-N voltage exceeds this voltage, a snubber circuit is necessary to absorb the surge under this voltage.
(3)	V_{CES}	The maximum sustained collector-emitter voltage of built-in IGBT and FWDi.
(4)	+/- I_C	The allowable continuous current flowing at collect electrode (Tc=25°C) Pulse width and period are limited due to junction temperature.
(5)	Tj	The maximum junction temperature rating of built-in power chips is 175°C(@Tc≤125°C). However, to ensure safe operation of DIPIPM, the average junction temperature should be limited to Tj(Ave)≤150°C (@Tc≤125°C). Repetitive temperature variation ΔTj affects the life time of power cycle, so please refer life time curves for safety design.
(6)	$V_{CC(PROT)}$	The maximum supply voltage for turning off IGBT safely in the case of an SC or OC faults. The power chip might not be protected and break down in the case that the supply voltage is higher than this specification.
(7)	Viso	Isolation voltage is the withstanding voltage between all terminals connected with conductive material and heatsink of heat radiation.
(8)	Tc position	Tc (case temperature) is defined to be the temperature just beneath the specified power chip. Please mount a thermocouple on the heat sink surface at the defined position to get accurate temperature information. Due to the control schemes such different control between P and N-side, there is the possibility that highest Tc point is different from above point. In such cases, it is necessary to change the measuring point to that under the highest power chip.

Power chips layout

Fig.2-1-1 indicates the position of the each power chips. (This figure is the view from laser marked side.)
In case of PSSxxNE1CT.

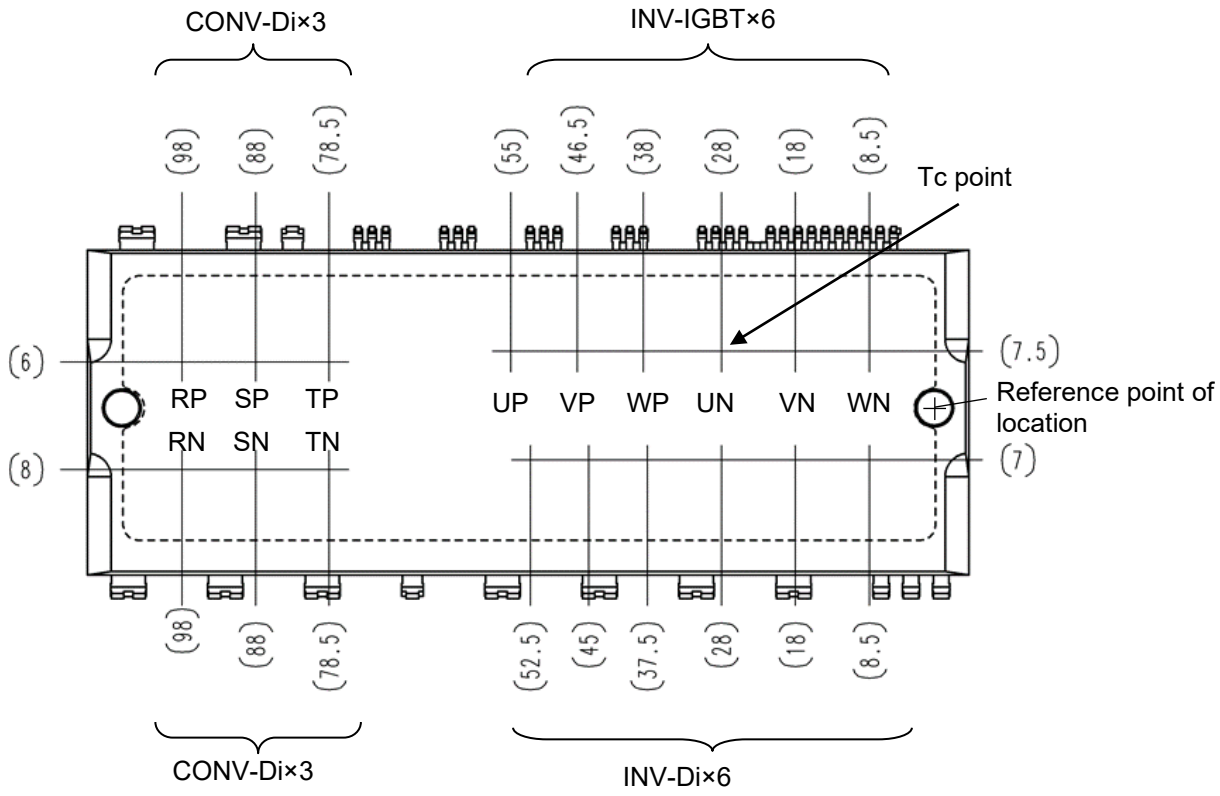


Fig. 2-1-1 Power chips layout (Unit : mm)

2.1.2 Thermal Resistance

Table 2-1-2 shows the thermal resistance between its chip junction and case.

Table 2-1-2. Thermal resistance of PSS50NE1CT (50A/1200V)

Symbol	Parameter	Condition	Limits			Unit
			Min.	Typ.	Max.	
$R_{th(j-c)Q}$	Junction to case thermal resistance (Note 1)	Inverter IGBT part (per 1/6 module)	-	-	0.65	K/W
$R_{th(j-c)F}$		Inverter FWD part (per 1/6 module)	-	-	1.10	
$R_{th(j-c)R}$		Converter part (per 1/6module)	-	-	1.00	

Note 1: Grease with good thermal conductivity and long-term endurance should be applied evenly with about +100μm~ +200μm on the contacting surface of DIPIPM and heat sink. The contacting thermal resistance between DIPIPM case and heat sink Rth(c-f) is determined by the thickness and the thermal conductivity of the applied grease. For reference, Rth(c-f) is about 0.25K/W (per 1chip, grease thickness: 20μm, thermal conductivity: 1.0W/m•K).

The above data shows static state thermal resistance. The thermal resistance goes into saturation in about 10 seconds. The unsaturated thermal resistance is called as transient thermal impedance which is shown in Fig.2-1-2. Zth(j-c)* is the normalized transient thermal impedance and formulation is described as Zth(j-c)*= Zth(j-c) / Rth(j-c)max. For example, the IGBT transient thermal impedance of PSS50NE1CT at 0.1s is 0.65×0.5=0.33K/W.

The transient thermal impedance isn't used for constantly current, but for short period current as millisecond order. (e.g. motor starting, motor lock･･･etc.)

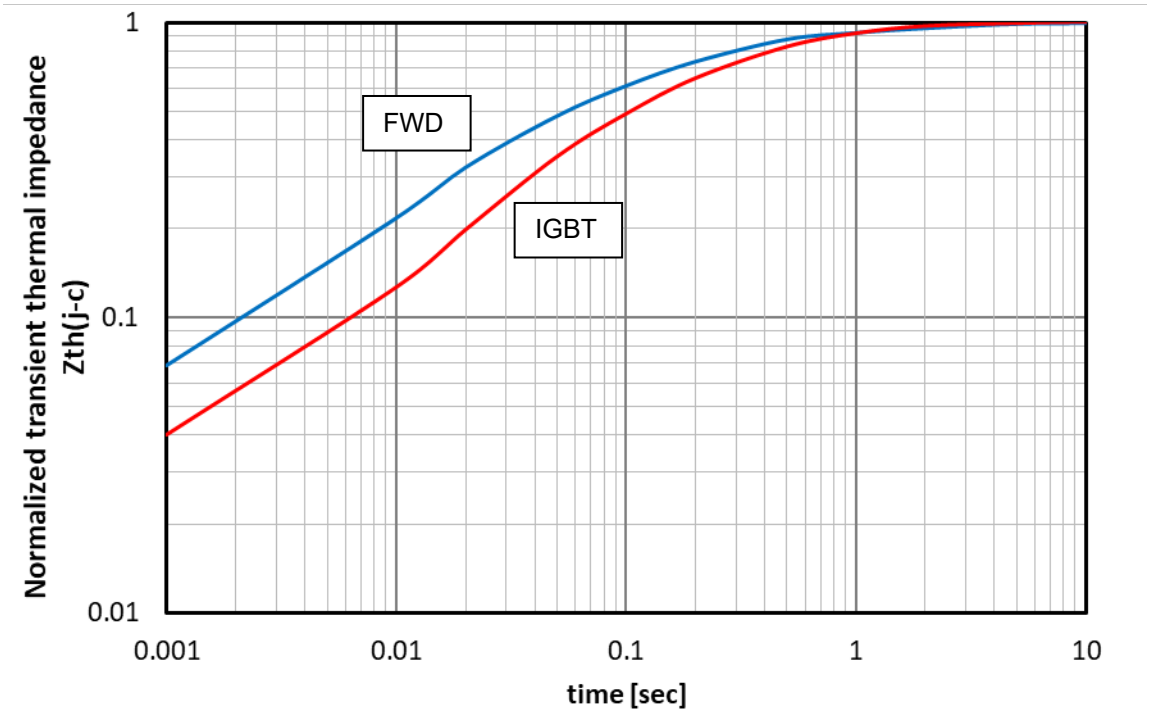


Fig. 2-1-2. Normalized transient thermal impedance

2.1.3 Electric Characteristics and Recommended Conditions

Table 2-1-3 shows the typical static characteristics and switching characteristics. (T_j = 25°C, unless otherwise noted)

Table 2-1-3 Static characteristics and switching characteristics of PSS50NE1CT(50A/1200V)

ELECTRICAL CHARACTERISTICS (T_j = 25°C, unless otherwise noted)

INVERTER PART

Symbol	Parameter	Condition		Limits			Unit
				Min.	Typ.	Max.	
$V_{CE(sat)}$	Collector-emitter saturation voltage	V_D=V_{DB} = 15V, V_{IN}= 5V	I_C= 50A, T_j= 25°C	-	1.50	1.90	V
			I_C= 50A, T_j= 125°C	-	1.80	2.30	
V_{EC}	FWDi forward voltage	V_{IN}= 0V, -I_C= 50A		-	1.85	2.40	V
t_{on}	Switching times	V_{CC}= 600V, V_D= V_{DB}= 15V I_C= 50A, T_j= 125°C, V_{IN}= 0↔5V Inductive Load (upper-lower arm)		1.40	2.30	3.30	µs
$t_{C(on)}$				-	0.40	0.85	µs
t_{off}				-	2.70	3.80	µs
$t_{C(off)}$				-	0.30	0.95	µs
t_{rr}				-	0.30	-	µs
I_{CES}	Collector-emitter cut-off current	V_{CE}=V_{CES}		-	-	1	mA

CONVERTER PART

Symbol	Parameter	Condition	Limits			Unit
			Min.	Typ.	Max.	
I_{RRM}	Repetitive reverse current	V_R=V_{RRM}	–	–	0.5	mA
V_F	Forward voltage drop	I_F=50A	–	1.20	1.65	V

Definition of switching time and performance test topology are shown in Fig.2-1-3 and 2-1-4.
Switching characteristics are measured by half bridge circuit with inductance load.

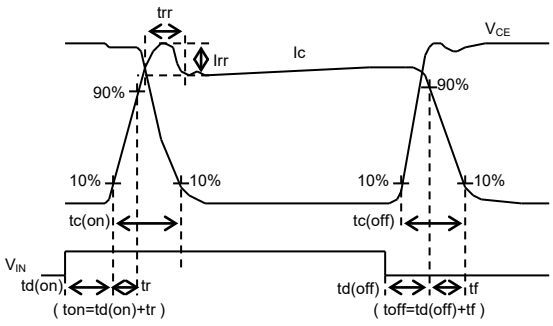


Fig. 2-1-3 Switching time definition

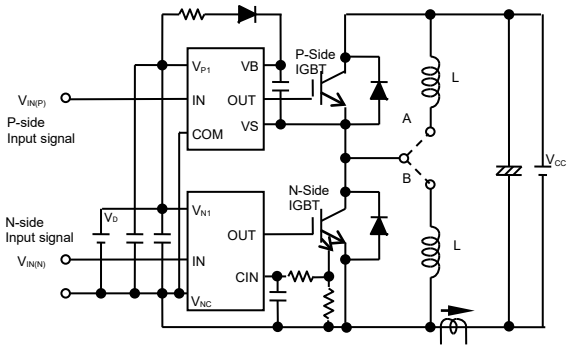


Fig. 2-1-4 Evaluation circuit (inductive load)

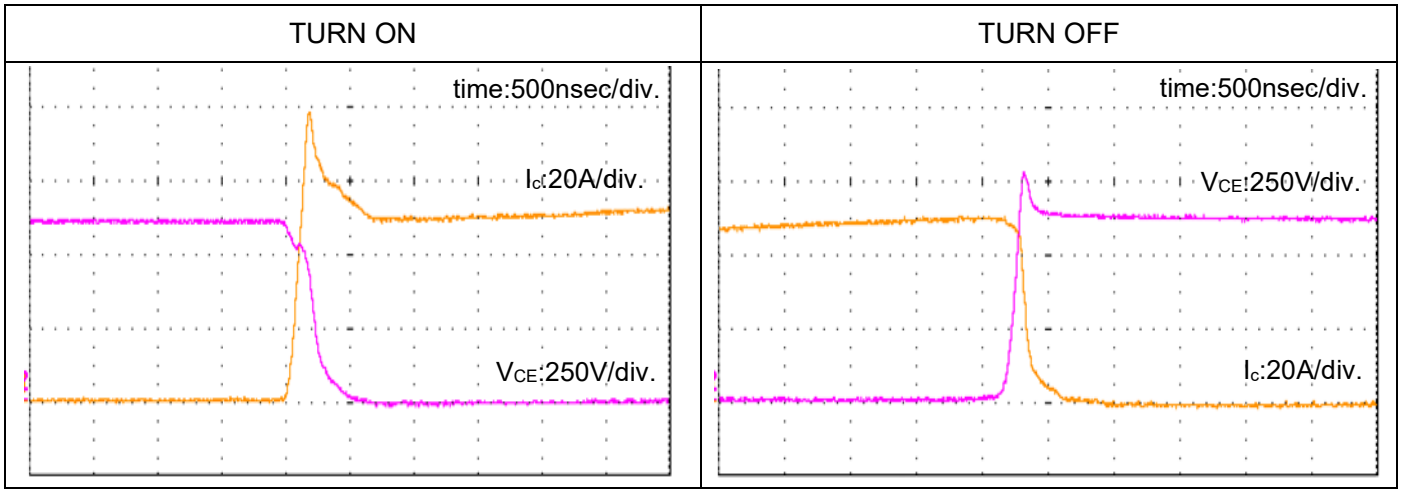


Fig. 2-1-5 Typical switching waveform for PSS50NE1CT (50A/1200V) inverter part
Condition: V_{CC}=600V, V_D=V_{DB}=15V, Ic=50A, Tj=125°C, inductive load half bridge circuit

Table 2-1-4 shows the typical control part characteristics. (T_j = 25°C, unless otherwise noted)

Table 2-1-4. Typical control part characteristics of PSS50NE1CT(50A/1200V)

CONTROL (PROTECTION) PART

Symbol	Parameter	Condition		Limits			Unit
				Min.	Typ.	Max.	
I_D	Circuit current	Total of V_{P1}-V_{NC}, V_{N1}-V_{NC}	V_D=15V, V_{IN}=0V	-	-	4.70	mA
			V_D=15V, V_{IN}=5V	-	-	4.70	
I_{DB}		Each part of V_{UFB}-V_{UFS}, V_{VFB}-V_{VFS}, V_{WFB}-V_{WFS}	V_D=V_{DB}=15V, V_{IN}=0V	-	-	2.40	
			V_D=V_{DB}=15V, V_{IN}=5V	-	-	2.40	
I_{SC}	Short circuit trip level	Rs= 46.4Ω (±1%), Without outer shunt resistors to NU,NV,NW terminals (Note 1)		75	-	-	A
UV_{DBt}	Control supply under-voltage protection(UV) for P-side of inverter part		Trip level	10.0	-	12.3	V
UV_{DBr}			Reset level	10.4	-	12.9	V
UV_{Dt}	Control supply under-voltage protection(UV) for N-side of inverter part and brake part		Trip level	10.3	-	12.5	V
UV_{Dr}			Reset level	10.8	-	13.0	V
V_{OT}	Temperature Output	Pull down R=5.1kΩ (Note 2)	LVIC Temperature=100°C	2.89	3.02	3.14	V
V_{FOH}	Fault output voltage	V_{SC} = 0V, F_O terminal pulled up to 5V by 10kΩ		4.9	-	-	V
V_{FOL}		V_{SC} = 1V, I_{FO} = 1mA		-	-	0.95	V
t_{FO}	Fault output pulse width	In case of C_{Fo}=22nF (Note 3)		1.6	2.4	—	ms
I_{IN}	Input current	V_{IN} = 5V		0.7	1.0	1.5	mA
$V_{th(on)}$	ON threshold voltage	Applied between U_P,V_P,W_P,U_N, V_N, W_N-V_{NC}		—	—	2.6	V
$V_{th(off)}$	OFF threshold voltage			0.8	—	—	

Note 1 : Short circuit protection detects sense current divided from main current at N-side IGBT only. In the case that outer shunt resistor is inserted into main current path, protection current level I_{SC} changes. For over -current protection by outside circuit, set the protection level under I_{CP}.

2 : DIPIPM doesn't shut down IGBTs and output fault signal automatically when temperature rises excessively. When temperature exceeds the protective level that user defined, controller (MCU) should stop immediately. Temperature of LVIC vs. V_{OT} output characteristics is described in Section 2.2.3. These minimum and maximum curves are based on theoretical designed value excluding LVIC temperature=100°C limits.

3 : Fault signal is output when short circuit or N-side control supply under-voltage protection works. The fault output pulse-width t_{FO} depends on the capacitance of C_{FO}. (C_{FO} (typ.) = t_{FO} x 9.1 x 10-6) [F])

Table 2-1-5 shows recommended operation conditions. Please apply and use under the recommended conditions to operate Large DIPIPM+ series safely. (T_j = 25°C, unless otherwise noted)

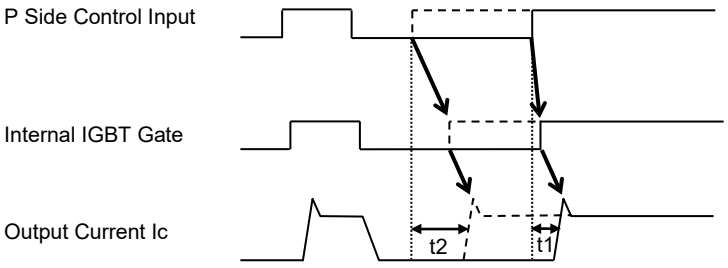
Table 2-1-5. Recommended operation conditions of PSS50NE1CT (50A/1200V)

RECOMMENDED OPERATION CONDITIONS

Symbol	Parameter	Condition	Limits			Unit
			Min.	Typ.	Max.	
V_{CC}	Supply voltage	Applied between P-NU,NV,NW	300	600	800	V
V_D	Control supply voltage	Applied between V_{P1}-V_{NC},V_{N1}-V_{NC}	13.5	15.0	16.5	V
V_{DB}	Control supply voltage	Applied between V_{UFB}-V_{UFS},V_{VFB}-V_{VFS},V_{WFB}-V_{WFS}	13.0	15.0	18.5	V
ΔV_D, ΔV_{DB}	Control supply variation		-1	-	1	V/μs
t_{dead}	Arm shoot-through blocking time	For each input signal	2.5	-	-	μs
f_{PWM}	PWM input frequency	T_C≤125°C, T_j≤150°C	-	-	20	kHz
PWIN(on)	Minimum input pulse width	(Note 1)	3.0	-	-	μs
PWIN(off)		(Note 2)	3.0	-	-	
V_{NC}	V_{NC} variation	Between V_{NC}- NU、NV、NW (including surge)	-5.0	-	+5.0	V

Note 1: DIPIPM might not make response if the input signal pulse width is less than PWIN(on).

2: DIPIPM might make no response or delayed response (P-side IGBT only) for input pulse width less than PWIN(off). Over rated collector current (Ic) operation, DIPIPM might make delayed response even if the input signal pulse width is PWIN(off) or more. The timing charts are described as below.



Real line: Normal response; turn on time t1
Broken line: Delayed response; turn on time t2
(t1: Normal switching time)

[note] About control supply variation

If high frequency noise superimposed to the control supply line, IC malfunction might happen and cause DIPIPM erroneous operation. To avoid such problem, line ripple voltage should meet the following specifications:

dV/dt ≤ +/-1V/μs, Vripple≤2Vp-p

2.1.4 Mechanical characteristics and specifications

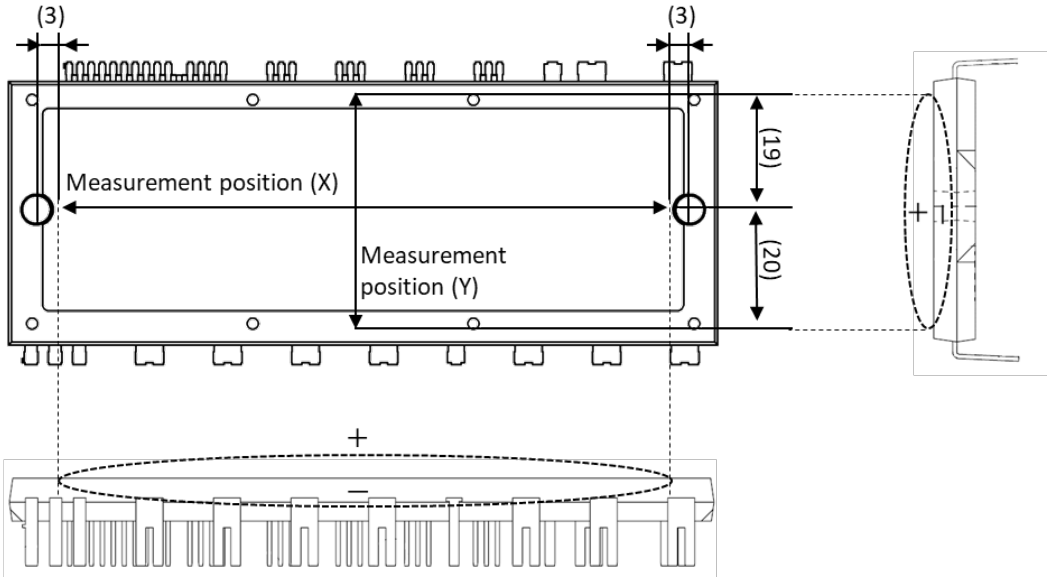
Table 2-1-6 shows mechanical characteristics and specifications. Please also refer section 2.4 for mounting instruction of Large DIPIPM+.

Table 2-1-6. Mechanical characteristics and specifications of PSS50NE1CT (50A/1200V)

MECHANICAL CHARACTERISTICS AND RATINGS

Parameter	Condition	Reference	Limits			Unit
			Min.	Typ.	Max.	
Mounting torque	Mounting screw : M4 (Note 1)	JEITA-ED-4701 402 method Ⅱ	0.98	1.18	1.47	N·m
Terminal strength pulling	Weight power terminal:40N control terminal:10N	JEITA-ED-4701 401 method Ⅰ	10	-	-	s
Terminal strength bending	Load 10N, 90deg. bend	JEITA-ED-4701 401 method Ⅲ	2	-	-	times
Weight			-	89	-	g
Heat radiation part flatness	(Note 2)		-50	-	130	μm

Note 1: Plain washers (ISO 7089~7094) are recommended.
2: Measurement positions of heat radiation part flatness are as below.

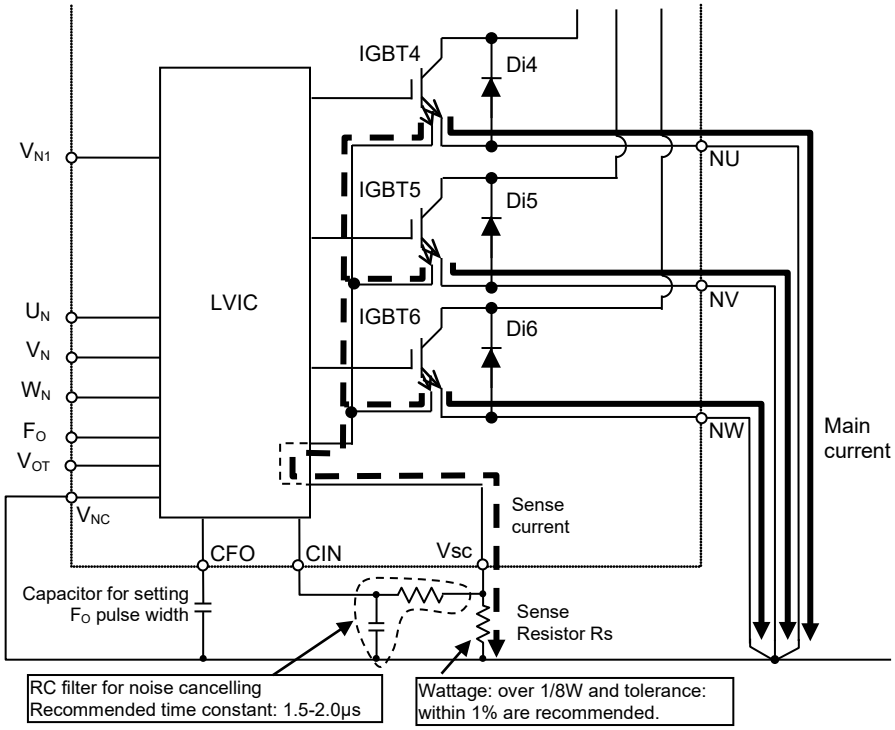


2.2 Protection functions and operating sequence

Large DIPIPM+ has two protection functions of short circuit (SC) and under voltage of control supply (UV). And it has also temperature output function of LVIC (V_{OT}). The operating principle and sequence are described as follows.

2.2.1 Short circuit protection

This series apply the detection method of small sense current, which is divided at N-side IGBT, to SC protection. So high wattage type shunt resistor isn't necessary for SC protection. (Fig.2-2-1)



*) This wattage of sense resistor is described as a guide, so it is recommended to evaluate on your real system well.

Fig.2-2-1 SC protection circuit

SC protection works by inputting the potential, which is generated by sense current flowing into the sense resistor, to the CIN terminal. Tabel 2-2-1 describes specified sense resistance and minimum SC protection current in that case for each products.

When SC ptotection works, DIPIPM shuts down all N-side IGBTs hardly and outputs Fo signal. Its pulse width(t_{Fo}) is set by C_{FO} capacitor ($C_{FO} = t_{FO} \times 9.1 \times 10^{-6}$ [F]).

To prvent malfunction, it is recommended to insert RC filter before inputting to CIN terminal and set the time constant to shut down withiin 2μs when short circuit occurs. (Time constant 1.5μ-2.0μs is recommended.) Also it is necessary to set the resistance of RC filter to ten or more times of the sense resistor Rs.(Hundred times is recommended.)

Table 2-2-1 SC protection trip level Tj=25°C (Not connecting outer shunt resistors to NU,NV,NW terminals.)

Type name	Rs	Min.
PSS100NE1CT	24.9Ω	120A
PSS75NE1CT	30.1Ω	112.5A
PSS50NE1CT	46.4Ω	75A
PSS35NE1CT	59.0Ω	52.5A

For sense resistor, its large fluctuation leads to large fluctuation of SC trip level. So it is necessary to select small variation and good temperature characteristic type (within +/-1% is recommended).

Wattage of the sense resistor can be estimated in view of the fact that the maximum split ratio between the main and sense currents is about 7000:1. (In this case maximum sense current flows.)

The estimation example for PSS50NE1CT is described as below.

[Estimation example]

(1) Normal operation state

It is assumed that the maximum main current for normal operation is 50A (rated current, for keeping a margin) and the sense resistance is 46.4Ω.

In this case, The maximum sense current flows through the sense resistor is calculated as below.

50A / 4000 = 12.5mA

And the loss at the sense resistor is

$P=I^2 \cdot R \cdot t=(12.5mA)^2 \times 46.4\Omega = 7.3mW$

(2) Short circuit state

When short circuit occures, its current depends on the condition, but up to IGBT saturation current (about 10 times of the rated current =350A) flows. So the sense current is

500A / 4000 = 125mA

But this current shut down within 2μs by SC protection. And the average loss at the sense resistor is

$P=I^2 \cdot R \cdot t= (125mA)^2 \times 46.4\Omega \times 2\mu s / 1s = 0.0015mW$

And drop voltage of this sense resistor is

V= 125mA x 46.4Ω= 5.8V

As explained above, over 0.03W wattage resistor will be suitable, but it is necessary to confirm on your real system finally.

[Remarks]

It takes more time (Table 2-2-2) from inputting over threshold voltage to CIN terminal to shutting down IGBTs. (Because of IC's transfer delay)

Table 2-2-2 Internal time delay of IC

Item	typ	max	Unit
IC transfer delay time	0.5	1.0	μs

Therefore, the total delay time from short circuit occurring to shutting down IGBTs is the sum of the delay by the outer RC filter and this IC delay.

[SC protection (N-side only)]

a1. Normal operation: IGBT ON and outputs current.
a2. Short circuit current detection (SC trigger) (It is recommended to set RC time constant 1.5~2.0μs so that IGBT shut down within 2.0μs when SC.)
a3. All N-side IGBTs' gates are hard interrupted.
a4. All N-side IGBTs turn OFF.
a5. Fo outputs with a fixed pulse width determined by the external capacitance C_{FO}.
a6. Input "L": IGBT off.
a7. Fo finishes output, but IGBTs don't turn on until inputting next ON signal (L→H).
(IGBT of each phase can return to normal state by inputting ON signal to each phase.)
a8. Normal operation: IGBT ON and outputs current.

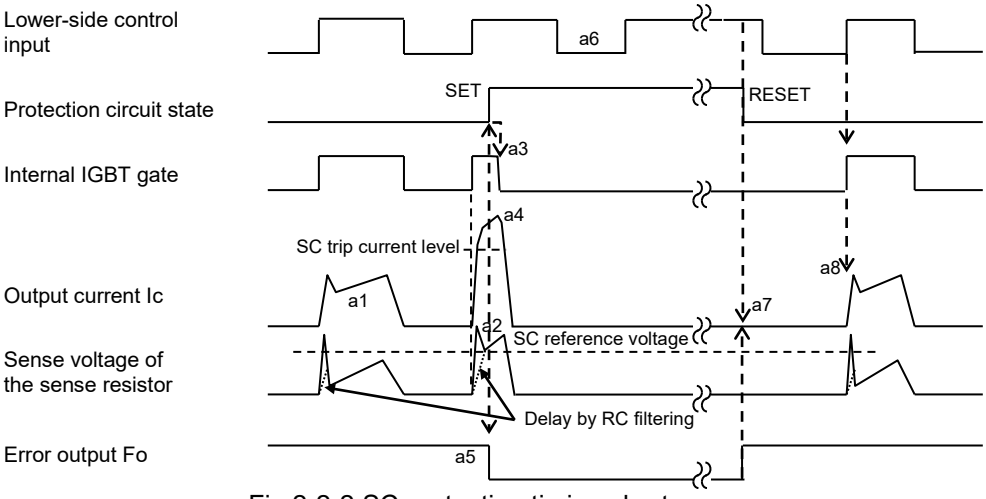


Fig.2-2-2 SC protection timing chart

2.2.2 Control Supply UV Protection

The UV protection is designed to prevent unexpected operating behavior as described in Table 2-2-3. Both P-side, N-side have UV protecting function. However fault signal(Fo) output only corresponds to N-side UV protection. Fo output continuously during UV state.

In addition, there is a noise filter (typ. 10μs) integrated in the UV protection circuit to prevent instantaneous UV erroneous trip. Therefore, the control signals are still transferred in the initial 10μs after UV happened.

Table 2-2-3 DIPIPM operating behavior versus control supply voltage

Control supply voltage (V_D, V_{DB})	Operating behavior
0-4V (P, N)	In this voltage range, built-in control IC may not work properly. Normal operating of each protection function (UV, Fo output etc.) is not also assured. Normally IGBT does not work. But external noise may cause DIPIPM malfunction (turns ON), so DC-link voltage need to start up after control supply starts-up.
4-UV_{Dt} (N), UV_{DBt} (P)	UV function becomes active and output Fo (N-side only). Even if control signals are applied, IGBT does not work.
UV_{Dt} (N)-13.5V UV_{DBt} (P)-13.0V	IGBT can work. However, conducting loss and switching loss will increase, and result extra temperature rise at this state,.
13.5-16.5V (N) 13.0-18.5V (P)	Recommended conditions.
16.5-20V (N) 18.5-20V (P)	IGBT works. However, switching speed becomes fast and saturation current becomes large at this state, increasing SC broken risk.
20V- (P, N)	The control circuit might be destroyed.

(note) Ripple Voltage Limitation of Control Supply

If high frequency noise superimposed to the control supply line, IC malfunction might happen and cause DIPIPM erroneous operation. To avoid such problem happens, line ripple voltage should meet the following specifications:

$dV/dt \leq +/-1V/\mu s$, $Vripple \leq 2Vp\text{-}p$

N-side UV Protection Sequence

a1. Control supply voltage V_D exceeds under voltage reset level (UV_{Dr}), but IGBT turns ON when inputting next ON signal (L→H).(IGBT of each phase can return to normal state by inputting ON signal to each phase.)
a2. Normal operation: IGBT turn on and carry current.
a3. V_D level drops to under voltage trip level. (UV_{Dt}).
a4. All N-side IGBTs turn OFF in spite of control input condition.
a5. Fo outputs for the period determined by the capacitance C_{FO}, but output is extended during V_D keeps below UV_{Dr}.
a6. V_D level reaches UV_{Dr}.
a7. Normal operation: IGBT ON and carry current.

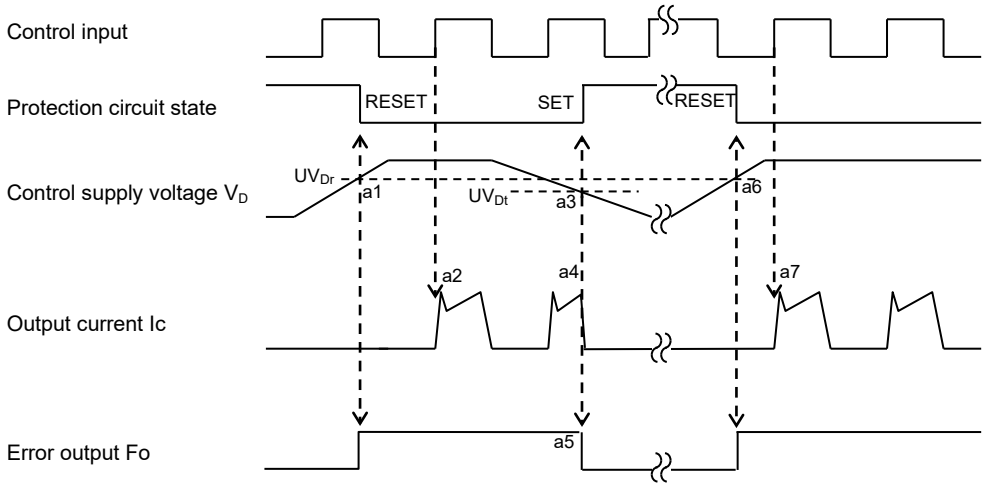


Fig.2-2-3 Timing chart of N-side UV protection

P-side UV Protection Sequence

b1. Control supply voltage V_{DB} rises. After the voltage reaches under voltage reset level UV_{DBr}, IGBT can turn on when inputting next ON signal (L→H).
b2. Normal operation: IGBT ON and outputs current.
b3. V_{DB} level drops to under voltage trip level (UV_{DBt}).
b4. IGBT of corresponding phase only turns OFF in spite of control input signal level, but there is no F_O signal output.
b5. V_{DB} level reaches UV_{DBr}.
b6. Normal operation: IGBT ON and carry current.

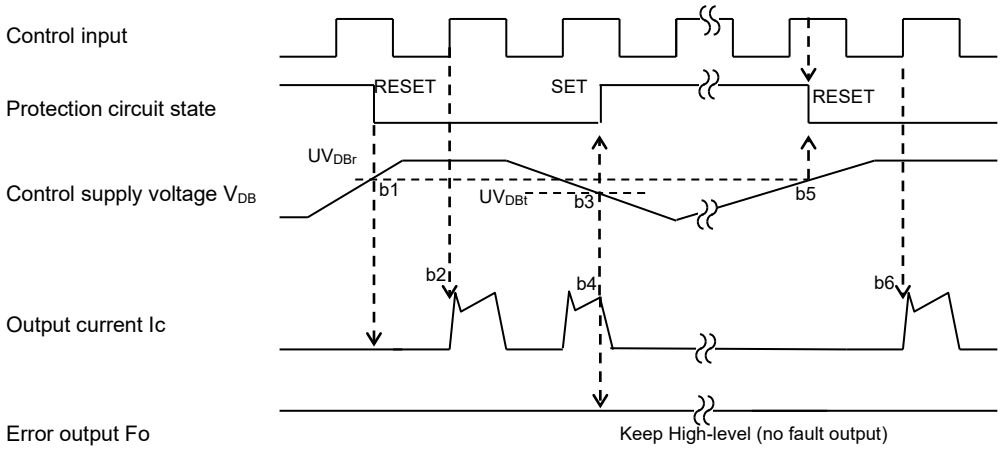


Fig.2-2-4 Timing Chart of P-side UV protection

2.2.3 Temperature output function V_{OT}

(1) Usage of this function

This function measures the temperature of control LVIC by built in temperature sensor on LVIC.

The heat generated at IGBT and FWDi transfers to LVIC through molding resin of package and outer heat sink. So LVIC temperature cannot respond to rapid temperature rise of those power chips effectively. (e.g. motor lock, short circuit). It is recommended to use this function for protecting from slow excessive temperature rise by such cooling system down and continuance of overload operation.（Replacement from the thermistor which was mounted on outer heat sink currently）

(note)

In this function, DIPIPM cannot shutdown IGBT and output fault signal by itself when temperature rises excessively. When temperature exceeds the defined protection level, controller (MCU) should stop the DIPIPM.

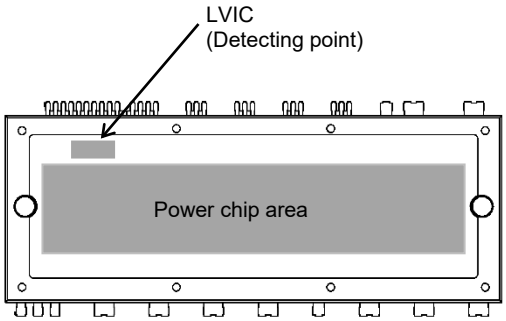


Fig.2-2-5 Temperature detecting point

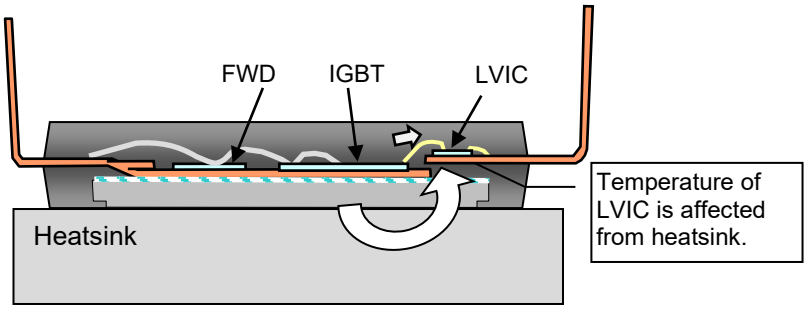


Fig.2-2-6 Thermal conducting from power chips

(2) V_{OT} characteristics

V_{OT} output circuit, which is described in Fig.2-2-7, is the output of OP amplifier circuit. The current capability of V_{OT} output is described as Table 2-2-4. The characteristics of V_{OT} output vs. LVIC temperature is linear characteristics described in Fig.2-2-9. There are some cautions for using this function as follows.

Table 2-2-4 Output capability

	min.
Source	1.7mA
Sink	0.1mA

Source: Current flow from V_{OT} to outside.
Sink : Current flow from outside to V_{OT}.

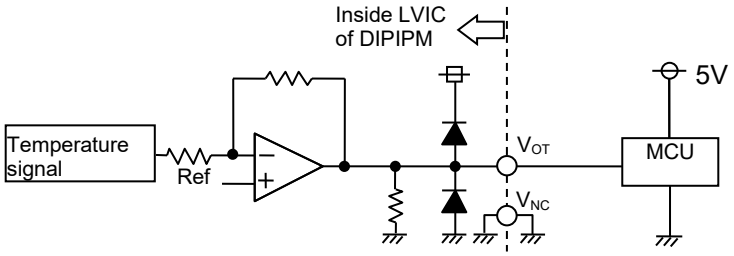


Fig.2-2-7 V_{OT} output circuit

(note) In the case of detecting lower temperature than room temperature

It is recommended to insert 5.1kΩ pull down resistor for getting linear output characteristics at lower temperature than room temperature. When the pull down resistor is inserted between V_{OT} and V_{NC}(control GND), the extra current calculated by V_{OT} output voltage / pull down resistance flows as LVIC circuit current continuously. In the case of only using V_{OT} for detecting higher temperature than room temperature, it isn't necessary to insert the pull down resistor.

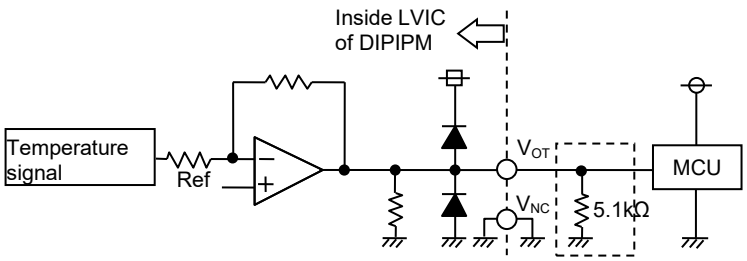


Fig.2-2-8 V_{OT} output circuit in the case of detecting low temperature

Please handle the following characteristics of V_{OT} output vs. LVIC temperature as reference data to set over temperature protection. These curves are based on theoretical designed value excluding specified value in the target specification.

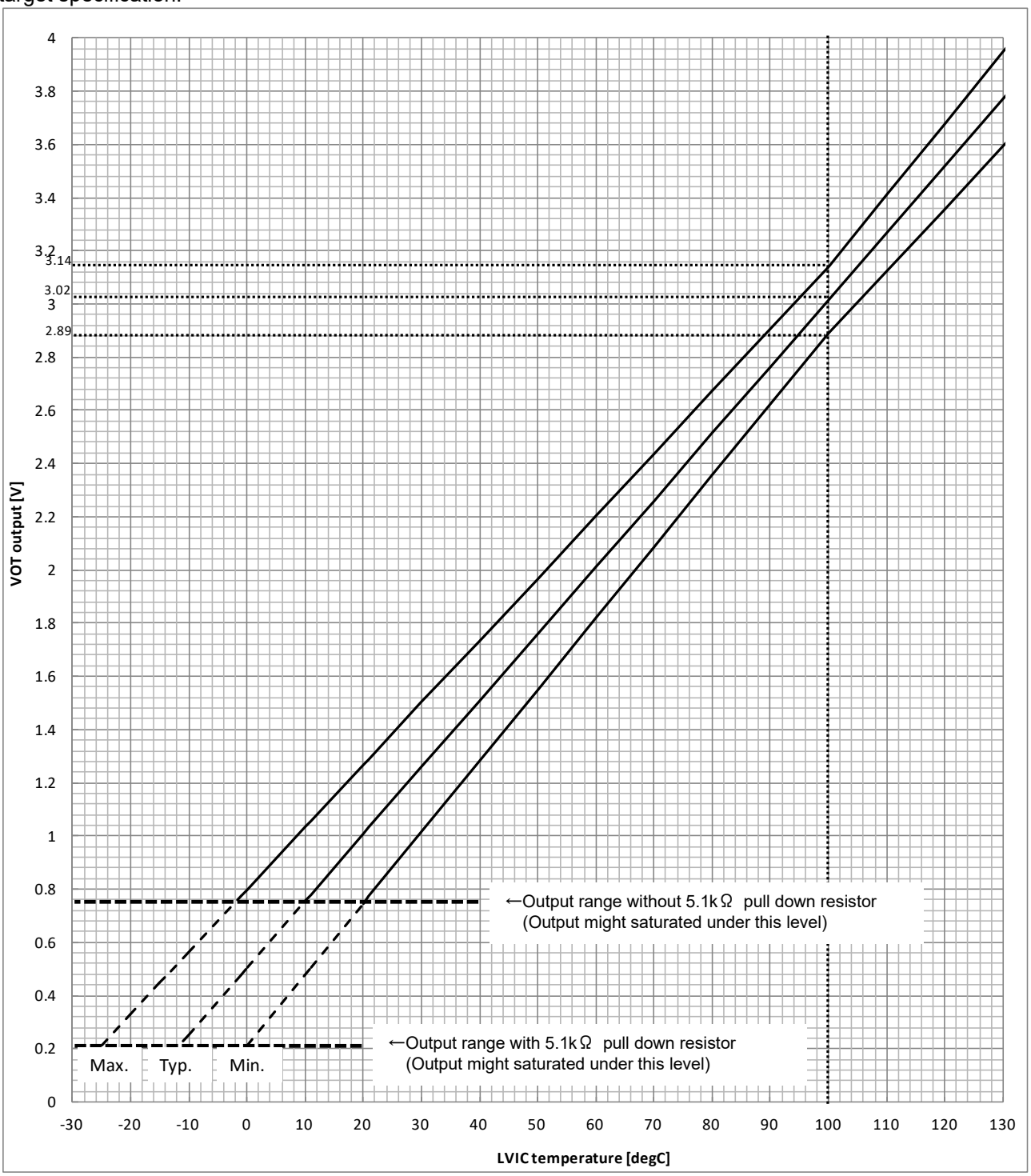


Fig.2-2-9 V_{OT} output vs. LVIC temperature

(These minimum and maximum curves are based on theoretical designed value excluding LVIC temperature=100°C limits.)

The heat of power chips transfers to LVIC through the heat sink and package, so the relationship between LVIC temperature: Tic(=V_{OT} output), case temperature: Tc(under the chip defined on datasheet), and junction temperature: Tj depends on the system cooling condition, heat sink, control strategy, etc.

This relationship may be different due to the cooling conditions. So when setting the threshold temperature for protection, it is necessary to get the relationship between them on your real system. And when setting threshold temperature Tic, it is important to consider the protection temperature assures; Tc≤125°C and Tj ≤150°C.

2.3 Package outline of DIPIPM+

2.3.1 Package outline

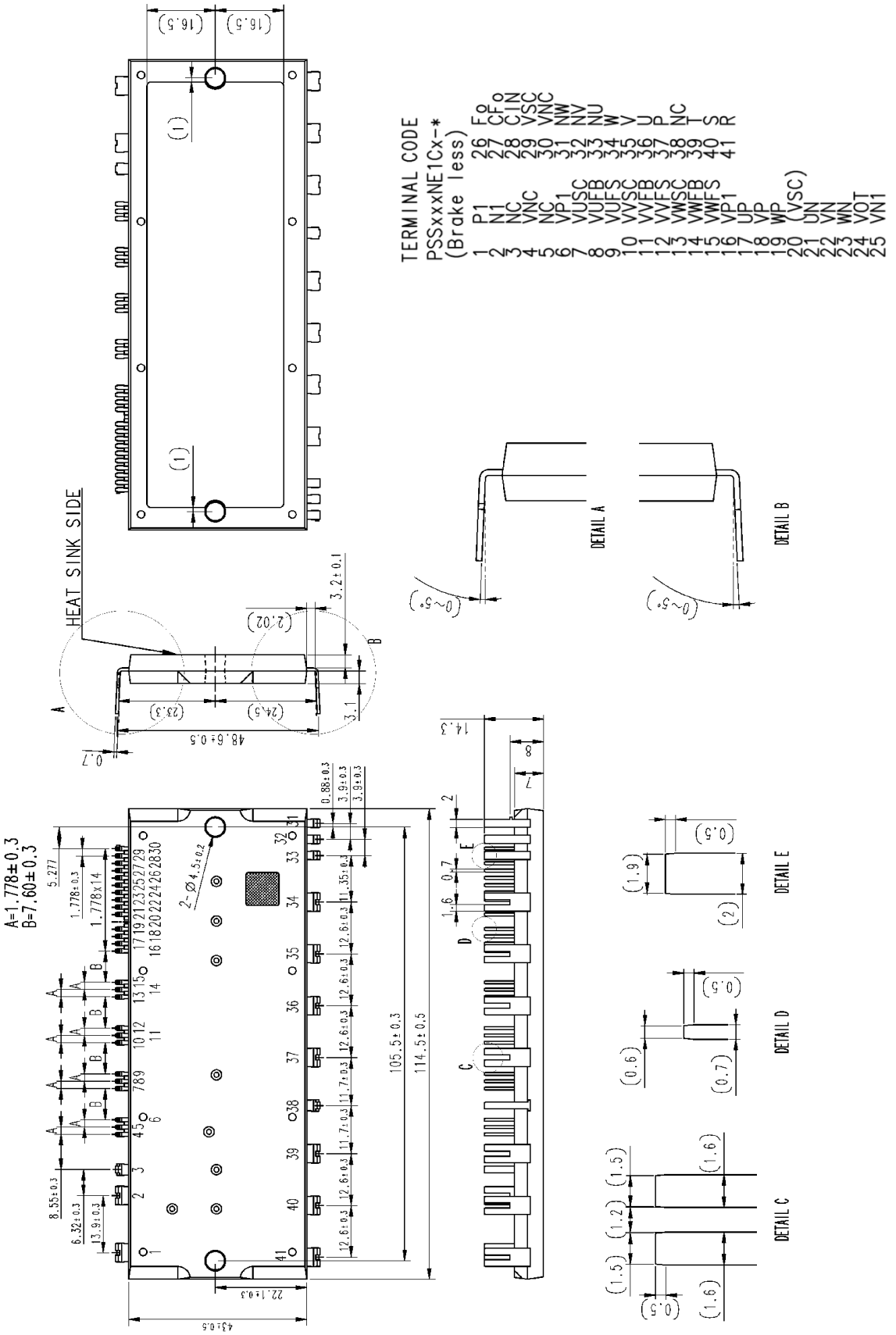


Fig. 2-3-1 Package outline drawing (Dimension in mm)

2.3.2 Marking

The laser marking specifications of Large DIPIPM+ is described in Fig.2-3-2. Company name, Country of origin, Type name, Lot number, and 2D code are marked on the surface of module.

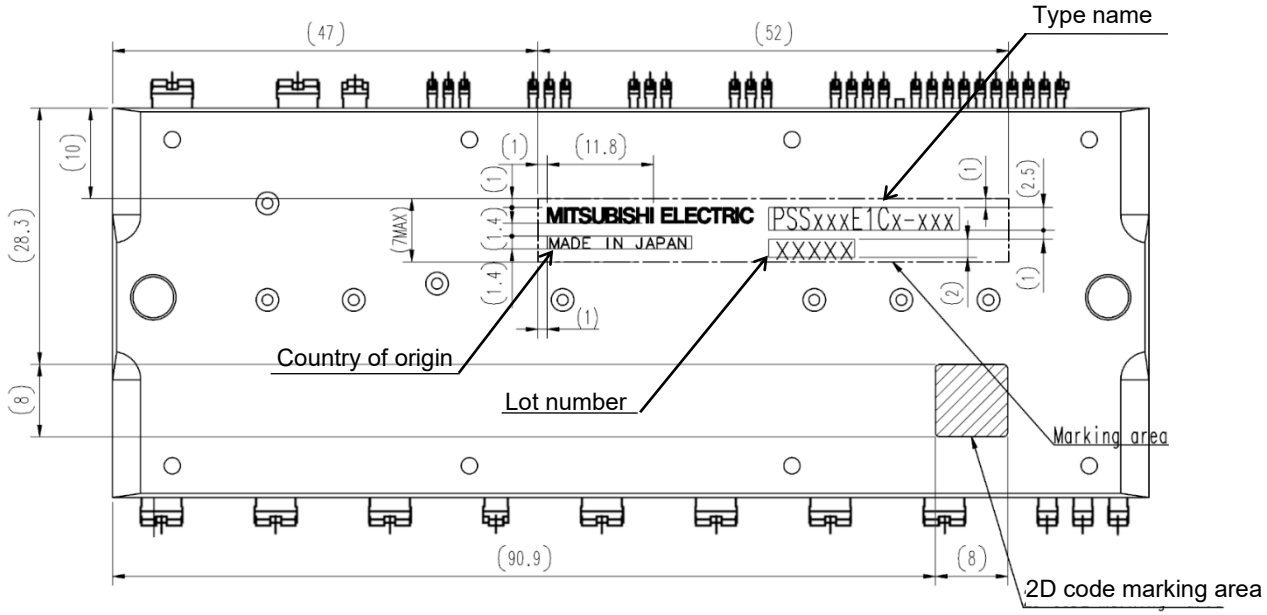


Fig.2-3-2 Laser marking view Large DIPIPM+ (Dimension in mm)

The Lot number indicates production year, month, running number and country of origin.
The detailed is described as below.

(Example) H 7 7 AA1

- Running number
- Product month (however O: October, N: November, D: December)
- Last figure of Product year (e.g. “5” in the case of 2015)
- Factory identification
  - H : Manufactured at the factory in China

2.3.3 Terminal Description

Table 2-3-1 Terminal Description

No.	Terminal	Description
1	P1	Output terminal for converter (+)
2	N1	Output terminal for converter (-)
3	(NC)	No connection
4	V_{NC}*1)	Control supply GND terminal
5	(NC)	No connection
6	V_{P1}*2)	Control supply positive terminal (+)
7	V_{USC}	Outside connect to UP drive supply GND terminal
8	V_{UFB}	U-phase P-side drive supply positive terminal
9	V_{UFS}	U-phase P-side drive supply GND terminal
10	V_{VSC}	Outside connect to VP drive supply GND terminal
11	V_{VFB}	V-phase P-side drive supply positive terminal
12	V_{VFS}	V-phase P-side drive supply GND terminal
13	V_{WSC}	Outside connect to WP drive supply GND terminal
14	V_{WFB}	W-phase P-side drive supply positive terminal
15	V_{WFS}	W-phase P-side drive supply GND terminal
16	V_{P1}*2)	Control supply positive terminal (+)
17	U_P	U-phase P-side control input terminal
18	V_P	V-phase P-side control input terminal
19	W_P	W-phase P-side control input terminal
20	(V_{SC})	No connection
21	U_N	U-phase N-side control input terminal
22	V_N	V-phase N-side control input terminal
23	W_N	W-phase N-side control input terminal
24	V_{OT}	Temperature output terminal
25	V_{N1}	N-side control supply positive terminal (+)
26	Fo	Fault signal output terminal
27	CFo	Fault pulse output width setting terminal
28	CIN	SC current trip voltage detecting terminal
29	V_{SC}	Sense current detecting terminal
30	V_{NC}*1)	GND terminal for brake control supply
31	NW	WN-phase IGBT emitter terminal
32	NV	VN-phase IGBT emitter terminal
33	NU	UN-phase IGBT emitter terminal
34	W	W-phase output terminal
35	V	V-phase output terminal
36	U	U-phase output terminal
37	P	Inverter DC-link positive terminal
38	(NC)	No connection
39	T	AC input terminal
40	S	AC input terminal
41	R	AC input terminal

(note)

1) Two V_{NC} terminals (GND terminal for control supply:4pin and 30pin) are connected mutually inside of Large DIPIPM+, please connect either terminal to GND and make the other terminal leave no connection.
2) Two V_{P1} terminals(6pin and 16pin) are connected mutually inside, please connect either terminal to supply and make the other terminal leave no connection.
3) Please connect V_{USC}-V_{UFS}(7-9pin), V_{VSC}-V_{VFS}(10-12pin), V_{WSC}-V_{WFS}(13-15pin).
4) Please no connection dummy terminal(3pin, 5pin,20pin and 38pin), because they may have electrical potential.

Table 2-3-2 Detailed description of input and output terminals

Item	Symbol	Description
P-side drive supply positive terminal P-side drive supply GND terminal	V_{UFB}- V_{UFS} V_{VFB}- V_{VFS} V_{WFB}- V_{WFS}	• Drive supply terminals for P-side IGBTs. • By mounting bootstrap capacitor, individual isolated power supplies are not needed for the P-side IGBT drive. Each bootstrap capacitor is charged by the N-side V_D supply when potential of output terminal is almost GND level. • Abnormal operation might happen if the V_D supply is not aptly stabilized or has insufficient current capability due to ripple or surge. In order to prevent malfunction, a bypass capacitor with favorable frequency and temperature characteristics should be mounted very closely to each pair of these terminals. • Inserting a Zener diode (24V/1W) between each pair of control supply terminals is helpful to prevent control IC from surge destruction.
Connect to P-side drive supply GND terminal	V_{USC}-V_{UFS} V_{VSC}-V_{VFS} V_{WSC}-V_{WFS}	• Each P-side V_{SC} terminal and each P-side drive supply GND terminal should be connected externally on PCB.
P-side control supply terminal N-side control supply terminal	V_{P1} V_{N1}	• Control supply terminals for the built-in HVIC and LVIC. • V_{P1}, and V_{N1} should be connected externally on PCB. In order to prevent malfunction caused by noise and ripple in the supply voltage, a bypass capacitor with good frequency characteristics should be mounted very close to these terminals. • Please design the supply carefully so that the voltage ripple caused by operation keep within the specification. ($dV/dt \leq +/-1V/\mu s$, $Vripple \leq 2$ Vp-p) • It is recommended to insert a Zener diode (24V/1W) between each pair of control supply terminals to prevent surge destruction.
N-side control GND terminal	V_{NC}	• Control ground terminal for the built-in HVIC and LVIC. • Please make sure that line current of the power circuit does not flow through this terminal in order to avoid noise influences. • Two V_{NC} terminals (GND terminal for control supply:4pin and 30pin) are connected mutually inside of Large DIPIPM+, please connect either terminal to GND and make the other terminal leave no connection.
Control input terminal	U_P,V_P,W_P U_N,V_N,W_N	• Control signal input terminals. This is Voltage input type. • These terminals are internally connected to Schmitt trigger circuit and pulled down by min 3.3kΩ resistor internally • The wiring of each input should be as short as possible to protect the DIPIPM from noise interference. • Please use RC coupling in case of signal oscillation. Pay attention to threshold voltage of input terminal, because input circuit has pull down resistor.
Sense current detect terminal	V_{SC}	• The sense current split at N-side IGBT flows out from this terminal. For SC protection, connect predefined resistor here.
Short-circuit trip voltage detecting terminal	CIN	• For short circuit protection, input the potential of external shuint resistor to CIN terminal through RC filter (for the noise immunity). • The time constant of RC filter is recommended to be up to 2μs.
Fault signal output terminal	F_O	• Fault signal output terminal for N-side abnormal state(SC or UV). • This output is open drain type. It is recommended to pull up F_O signal line to the 5V supply by 10kΩ when Fo signal is input to MCU directly (Check whether the V_{FO} satisies the threshold level of input of MCU when selecting resistance). • In the case of directly driving opto coupler by Fo output it is needed to set the pull-up resistance so that I_{FO} becomes under 5mA(maximum rating). And pulled up to 15V supply is recommended.(V_{FO} increases in propotion to increasing I_{FO}.)
Fault pulse output width setting terminal	C_{FO}	• The terminal is for setting the fault pulse output width. • An external capacitor should be connected between this terminal and V_{NC}. When 22nF capacitor is connected, then the Fo pulse width becomes 2.4ms. Because of $C_{FO} = t_{FO} \times 9.1 \times 10^{-6}$ (F)
Temperature output terminal	V_{OT}	• LVIC temperature is ouput by analog signal. It is ouput of OP amplifer internally. • It is recommended to connect 5.1kΩ pulldown resistor if output linearlity is necessary under room temperature.

(Continue)

Item	Symbol	Description
Inverter DC-link positive terminal	P	• DC-link positive power supply terminal. • Internally connected to the collectors of all P-side IGBTs. • To suppress surge voltage caused by DC-link wiring or PCB pattern inductance, smoothing capacitor should be inserted very closely to the P terminal. It is also effective to add small film capacitor with good frequency characteristics for snubber.
Inverter DC-link negative terminal	NU, NV, NW	• Emitter terminal of each N-side IGBT • If common emitter circuit (one shunt control) is applied, connect these terminals together at the point as close from the package as possible. • Each power GND pattern inductance should be less than 10nH.
Inverter power output terminal	U, V, W	• Inverter output terminals for connection to inverter load (e.g. AC motor). • Each terminal is internally connected to the intermidiate point of the corresponding IGBT half bridge arm.
AC power supply input terminal	R, S, T	• AC power supply input terminal
Converter positive output terminal	P1	• Converter positive output terminal
Converter GND terminal	N1	• Converter GND terminal

(note)

Use oscilloscope to check voltage waveform of each power supply terminals and P and N terminals, the time division of OSC should be set to about 1μs/div. Please ensure the voltage (including surge) not exceed the specified limitation.

If there is a surge more than threshold of ratings or superimposed noise, it is necessary to take some counter noise measurements; revising pattern, replacing capacitor, apply zener diode, enhancing filtering and so on.

2.4 Mounting Method

This section are described the electric spacing and mounting precautions of Large DIPIPM+.

2.4.1 Electric Spacing of Large DIPIPM+

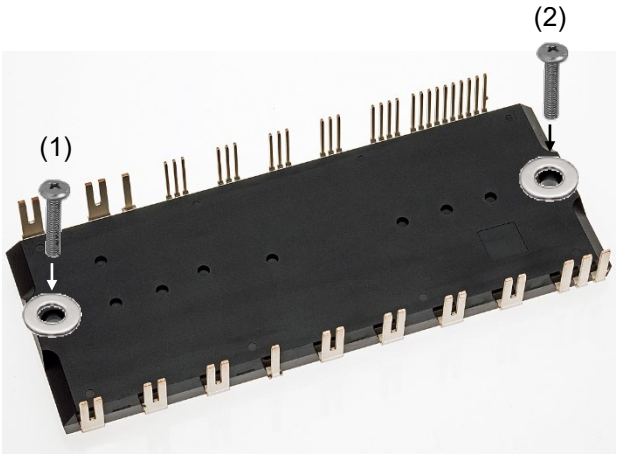
The electric spacing specification of Large DIPIPM+ is shown in Table 2-4-1.

Table 2-4-1 Minimum insulation distance(minimum value)

Clearance(mm)		Creepage(mm)	
Between power terminals	7.4	Between power terminals	7.9
Between control terminals	6.1	Between control terminals	6.5
Between terminals and heat sink	3.1	Between terminals and heat sink	3.1

2.4.2 Mounting Method and Precautions

When installing the module to the heat sink, excessive or uneven fastening force might apply stress to inside chips. Then it will lead to a broken or degradation of the chips or insulation structure. The recommended fastening procedure is shown in Fig.2-4-1. When fastening, it is necessary to use the torque wrench and fasten up to the specified torque. And pay attention not to have any foreign particle on the contact surface between the module and the heat sink. Even if the fixing of heatsink was done by proper procedure and condition, there is a possibility of damaging the package because of tightening by unexpected excessive torque or tucking particle. For ensuring safety it is recommended to conduct the confirmation test (e.g. insulation inspection) on the final product after fixing the DIPIPM with the heatsink.



Temporary fastening
(1)→(2)

Permanent fastening
(1)→(2)

Note: Generally, the temporary fastening torque is set to 20-30% of the maximum torque rating.
Not care the order of fastening (1) or (2), but need to fasten alternately.

Fig.2-4-1 Recommended screw fastening order

Table 2-4-2 Mounting torque and heat sink flatness specifications

Item	Condition	Min.	Typ.	Max.	Unit
Mounting torque	Screw : M4	0.98	1.18	1.47	N·m
Flatness of outer heat sink	Refer Fig.2-4-2	-50	―	100	μm

(note): Recommend to use plain washer (ISO7089-7094) in fastening the screws.

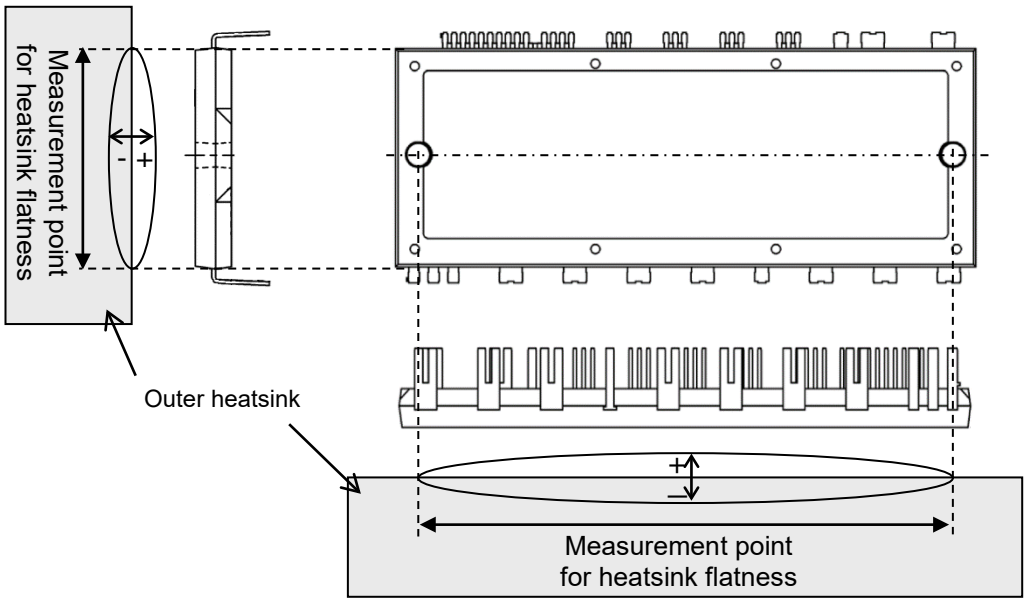


Fig.2-4-2 Measurement point of heat radiation part flatness

In order to get effective heat dissipation, it is necessary to enlarge the contact area as much as possible to minimize the contact thermal resistance. Regarding the heat sink flatness (warp/concavity and convexity) on the module installation surface, the surface finishing-treatment should be within Rz12.

Evenly apply thermally-conductive grease with 100μ-200μm thickness over the contact surface between a module and a heat sink, which is also useful for preventing corrosion. Furthermore, the grease should be with stable quality and long-term endurance within wide operating temperature range. The contacting thermal resistance between DIPIPM case and heat sink $R_{th(c-f)}$ is determined by the thickness and the thermal conductivity of the applied grease. For reference, $R_{th(c-f)}$ is about 0.25K/W (per chip, grease thickness: 20μm, thermal conductivity: 1.0W/m·k). When applying grease and fixing heat sink, pay attention not to take air into grease. It might lead to make contact thermal resistance worse or loosen fixing in operation.

Pay attention to the selection of thermal conductive grease. The grease thickness after fixing the heatsink may increase due to the properties of the grease (contained filler diameter, viscosity, amount of application and so on). And it may cause increase of contact thermal resistance or package crack. Please contact thermal conductive grease manufacturer for its detailed characteristics.

2.4.3 Soldering Conditions

The recommended soldering condition is mentioned as below.
(Note: The reflow soldering cannot be recommended for DIPIPM.)

(1) Flow (wave) Soldering

DIPIPM is tested on the condition described in Table 2-4-3 about the soldering thermostability, so the recommended conditions for flow (wave) soldering are soldering temperature is up to 265°C and the immersion time is within 11s.

The actual condition might need some adjustment based on its flow condition of solder, the speed of the conveyer, the land pattern and the through hole shape on the PCB, etc. It is necessary to confirm whether it is appropriate or not for your real PCB finally..

Table 2-4-3 Reliability test specification

Item	Condition
Soldering thermostability	260±5°C, 10±1s

(2) Hand soldering

Since the temperature impressed upon the DIPIPM may changes based on the soldering iron types (wattages, shape of soldering tip, etc.) and the land pattern on PCB, the unambiguous hand soldering condition cannot be decided.

As a general requirement of the temperature profile for hand soldering, the temperature of the root of the DIPIPM terminal should be kept less than 150°C for considering glass transition temperature (Tg) of the package molding resin and the thermal withstand capability of internal chips. Therefore, it is necessary to check the DIPIPM terminal root temperature, solderability and so on in your real PCB, when configure the soldering temperature profile. (It is recommended to set the soldering time as short as possible.)

Large DIPIPM+ Series Application note

CHAPTER 3 : SYSTEM APPLICATION GUIDANCE

3.1 Application guidance

This chapter states the DIPIPM+ application method and interface circuit design hints.

3.1.1 System connection

C1: Electrolytic type with good temperature and frequency characteristics
Note: the capacitance also depends on the PWM control strategy of the application system
C2: 0.1μ-2μF ceramic capacitor with good temperature, frequency and DC bias characteristics
C3: More than 1μF Film capacitor (for snubber)
D1: Zener diode 24V/1W for surge absorber

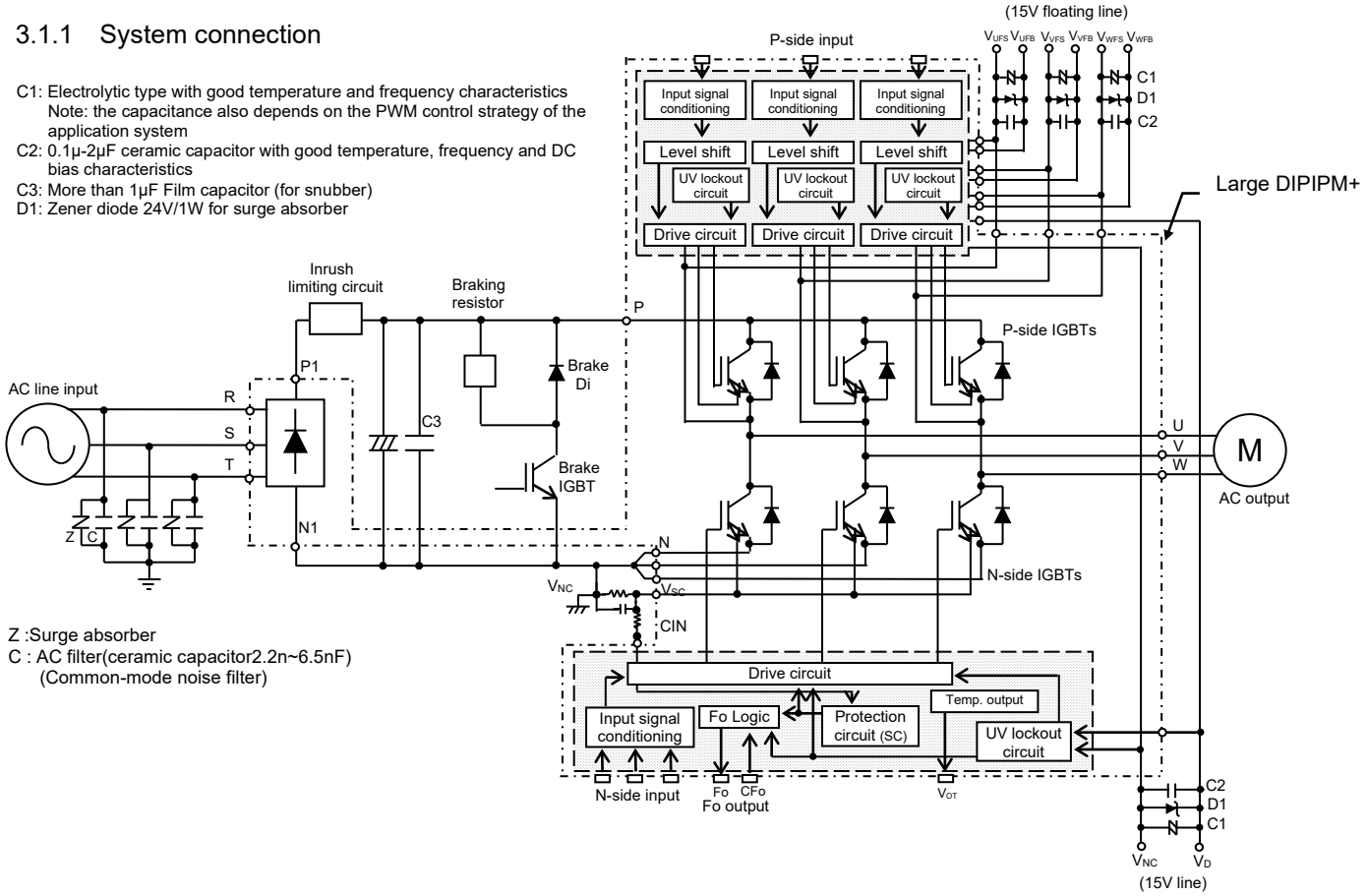


Fig.3-1-1 System block diagram (Example)

3.1.2 Interface Circuit (Direct Coupling Interface example)

Fig.3-1-2 shows a typical application circuit of interface schematic, in which control signals are transferred directly input from a controller (e.g. MCU).

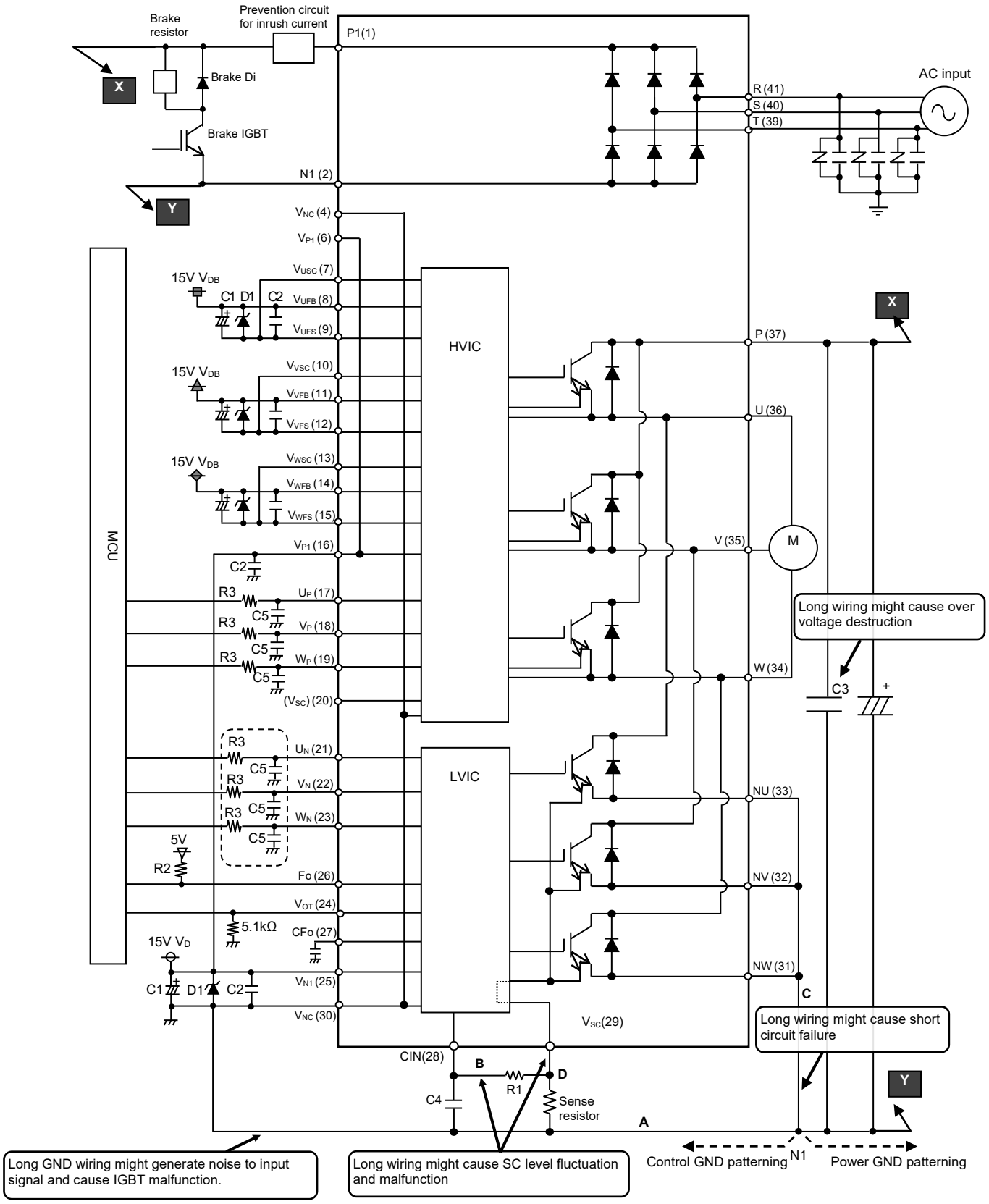


Fig.3-1-2 Interface circuit example(Direct coupling)

Note for the previous application circuit:

1 :If control GND and power GND are patterned by common wiring, it may cause malfunction by fluctuation of power GND level. It is recommended to connect control GND and power GND at only a N1 point at which NU, NV, NW are connected to power GND line.
2 :It is recommended to insert a Zener diode D1 (24V/1W) between each pair of control supply terminals to prevent surge destruction.
3 :To prevent surge destruction, the wiring between the smoothing capacitor and the P, N1 terminals should be as short as possible. Also, insert a snubber capacitor C3 of appropriate capacity (1μF or more) between the P-N1 terminals. Please design the capacity of the snubber capacitor so that it is optimized according to the wiring pattern etc..
4 :R1, C4 of RC filter for preventing protection circuit malfunction is recommended to select tight tolerance, temp-compensated type. The time constant R1C4 should be set so that SC current is shut down within 2μs. (1.5μs~2μs is general value.) SC interrupting time might vary with the wiring pattern, so the enough evaluation on the real system is recommended. If R1 is too small, it may leads to delay of protection. So R1 should be min. 10 times larger resistance than Rs. (100 times is recommended.)
5 :To prevent erroneous operation, the wiring of A, B, C should be as short as possible.
6 :For sense resistor, the variation within 1%(including temperature characteristics), low inductance type is recommended. And the over 0.03W is recommended, but it is necessary to evaluate in your real system finally.
7 :To prevent erroneous SC protection, the wiring from V_{SC} terminal to CIN filter should be divided at the point D that is close to the terminal of sense resistor. And the wiring should be patterned as short as possible.
8 :All capacitors should be mounted as close to the terminals of the DIPIPM as possible. (C1: good temperature, frequency characteristic electrolytic type, and C2: 0.1μ~2.0μF, good temperature, frequency and DC bias characteristic ceramic type are recommended.)
9 :Input drive is High-active type. There is a min. 3.3kΩ pull-down resistor in the input circuit of IC. To prevent malfunction, the wiring of each input should be as short as possible. And it is recommended to insert RC filter (e.g. R3=100Ω and C5=1000pF) and confirm the input signal level to meet the turn-on and turn-off threshold voltage. Thanks to HVIC inside the module, direct coupling to MCU without any opto-coupler or transformer isolation is possible.
10 :Fo output is open drain type. Fo output will be max 0.95V(@I_{FO}=1mA,25°C), so it should be pulled up to MCU or control power supply (e.g. 5V,15V) by a resistor that makes I_{Fo} up to 1mA. (In the case of pulled up to 5V, 10kΩ is recommended.)
11 :Error signal output width (t_{Fo}) can be set by the capacitor connected to C_{FO} terminal. C_{FO}(typ.) = t_{Fo} x 9.1 x 10^{-6} (F)
12 :If high frequency noise superimposed to the control supply line, IC malfunction might happen and cause erroneous operation. To avoid such problem, voltage ripple of control supply line should meet dV/dt ≤+/-1V/μs, Vripple≤2Vp-p.
13 :For DIPIPM, it isn't recommended to drive same load by parallel connection with other phase IGBT or other DIPIPM.
14 :No.4 and No.30 V_{NC} terminals (GND terminal for control supply) are connected mutually inside of DIPIPM+ and also No.6 and No.16 V_{P1} terminals are connected mutually inside, please connect either No.4 or No.30 terminal to GND and also connect either No.6 or No.16 terminal to supply and make the unused terminal leave no connection.
15 :Please connect the V_{USC}-V_{UFS}(7-9 terminal)、V_{VSC}-V_{VFS}(10-12 terminal)、V_{WSC}-V_{WFS}(13-15terminal) externally.
16 :Although 3, 5, 20 and 38 terminals are dummy terminals, it may have an electric potential, so make it a no connection.

3.1.3 Interface circuit (example of opto-coupler isolated interface)

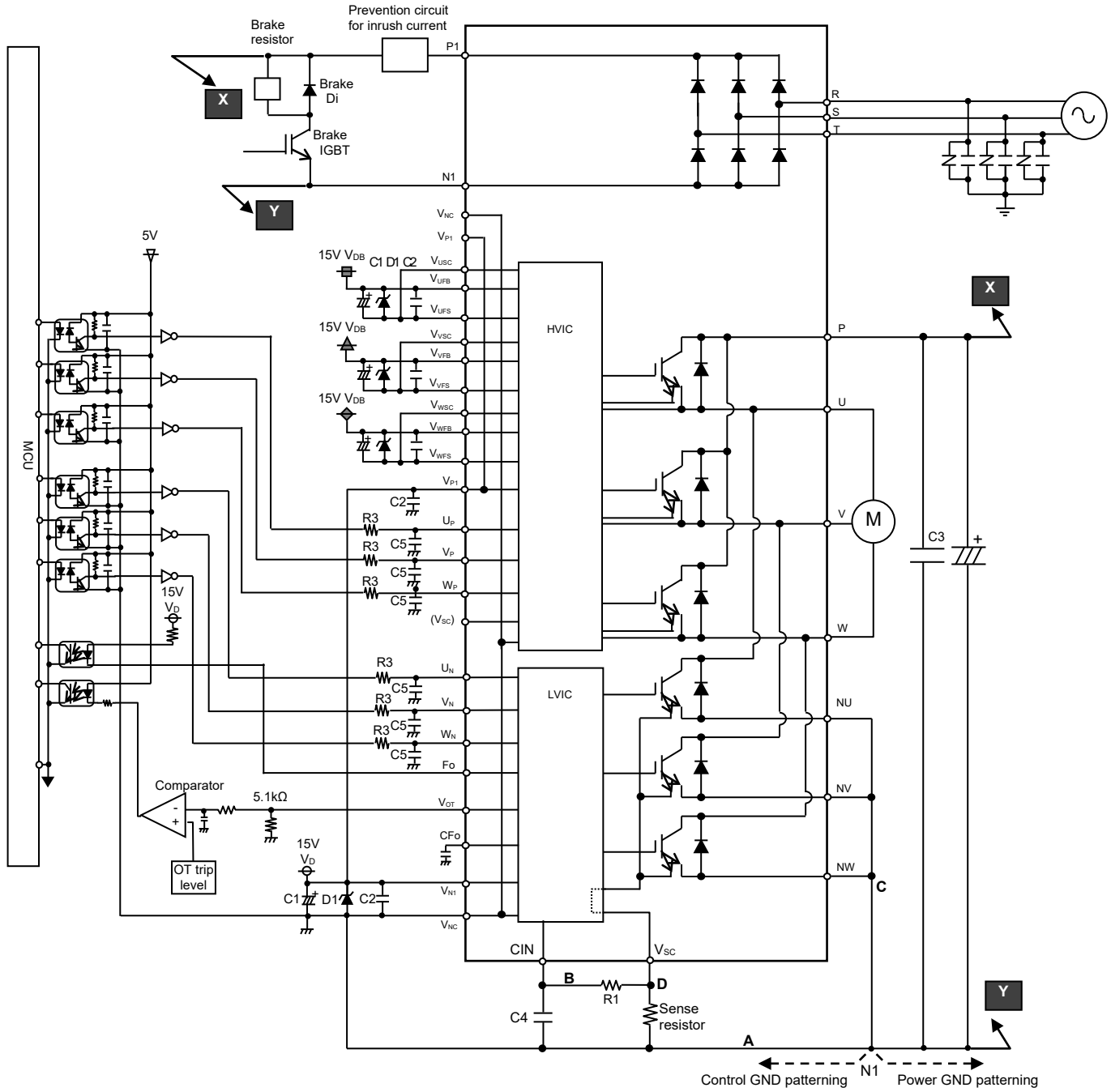


Fig.3-1-3 Interface circuit example with opto-coupler

(note)

(1) High speed (high CMR) opto-coupler is recommended.

(2) Set the current limiting resistance to make Fo sink current I_{FO}=5mA or less when the opto-coupler is driven by Fo output directly. To assure I_{FO}=5mA, it will be needed to pull up to 15V supply since Fo output may be max 4.75V (@I_{FO}=5mA, 25°C).

(3) To prevent malfunction, it is strongly recommended to insert RC filter (e.g. R3=100Ω and C5=1000pF) and confirm the input signal level to meet turn-on and turn-off threshold voltage.

(4) About comparator circuit at V_{OT} output, it is recommended to design the input circuit with hysteresis because of preventing output chattering.

3.1.4 Circuits of Signal Input Terminals and Fo Terminal

(1) Internal Circuit of Control Input Terminals

DIPIPM is high-active input logic. 3.3kΩ(min) pull-down resistor is built-in each input circuits of the DIPIPM as shown in Fig.3-1-4 , so external pull-down resistor is not needed.

Furthermore, the turn-on and turn-off threshold voltage of input signal are as shown in Table 3-1-1 .

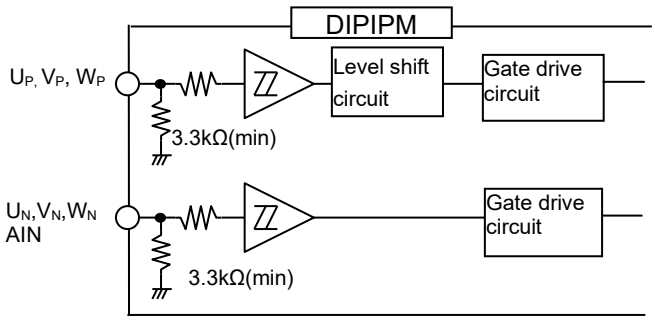


Fig.3-1-4 Internal structure of control input terminals

Table 3-1-1 Input threshold voltage ratings(Tj=25°C)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Turn-on threshold voltage	Vth(on)	U_P,V_P,W_P-V_{NC} terminals,	–	–	2.6	V
Turn-off threshold voltage	Vth(off)	U_N,V_N,W_N-V_{NC} terminals,	0.8	–	–	

(note)

(1) The wiring of each input should be patterned as short as possible. If the pattern is long and the noise is imposed on the pattern (e.g. Fig3-1-5), it may be effective to insert RC filter.

(2) There are limits for the minimum input pulse width in the DIPIPM. The DIPIPM might make no response or delayed response, if the input pulse width (both on and off) is shorter than the specified value. (Table 3-1-2)

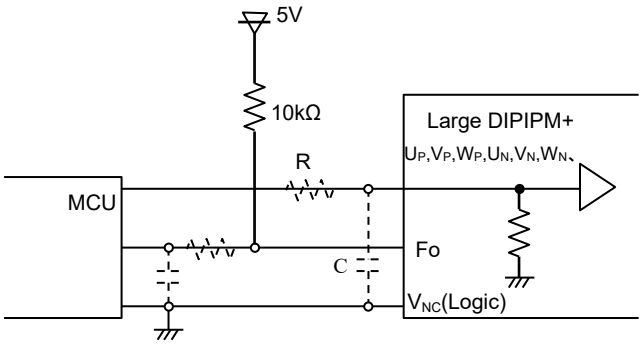


Fig.3-1-5 Control input connection

(note)

(1) The RC coupling (parts shown as broken line) at each input depends on user's PWM control strategy and the wiring impedance of the printed circuit board.

(2) The DIPIPM signal input section integrates a 3.3kΩ(min) pull-down resistor. Therefore, when using an external filtering resistor, please be careful to the signal voltage drop at input terminal.

Table 3-1-2 Allowable minimum input pulse width

Item	Symbol	Condition	Min. value	Unit
Allowable minimum input pulse width	PWIN(on)		3.0	μs
	PWIN(off)		3.0	

(note)

(1) DIPIPM might not make response if the input signal pulse width is less than PWIN(on).

(2) DIPIPM might make no response or delayed response (P-side IGBT only) for input pulse width less than PWIN(off). Over rated collector current (Ic) operation, DIPIPM might make delayed response even if the input signal pulse width is PWIN(off) or more. The timing charts are described as below.

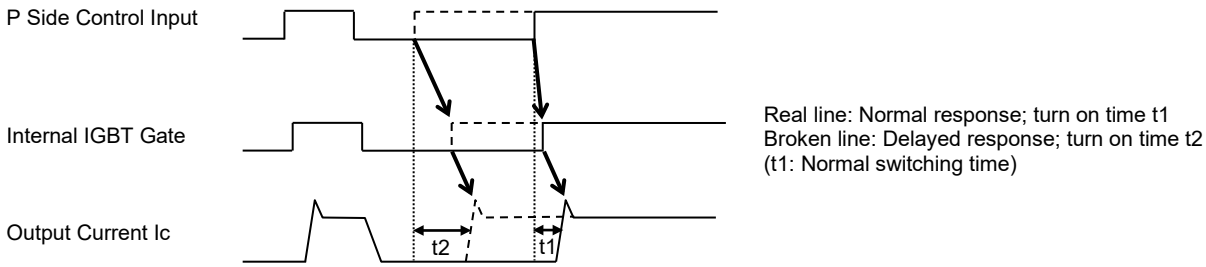


Fig.3-1-6 Delayed response of output operation with inputting less than PWIN(OFF) for P-side

(2) Internal circuit of Fo terminal

Fo terminal is an open drain type. When Fo output is input into MCU(controller) directly, it is necessary to note the dependency of V_{FO} on I_{FO} (V_{FO}=max0.95V @I_{FO}=1mA, 25°C) and set pull up resistance so that Fo signal level fits to the input threshold voltage of MCU. In the case of pulling up to 5V supply, it is recommended to pull up by 10kΩ resistor.

When the opto-coupler is driven by Fo output directly, the maximum Fo sink current becomes 5mA or less. To assure I_{FO}=5mA, it will be needed to pull up to 15V supply since Fo output may be max 4.75V (@I_{FO}=5mA, 25°C).

If max 5mA coupler driving current is not enough, it is necessary to apply buffer circuit for increasing driving current.

Fig. 3-1-7 shows the typical V-I characteristics of Fo terminal.

Table 3-1-3 Electric characteristics of Fo terminal.

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Fault output voltage	V_{FOH}	V_{SC}=0V, Fo=10kΩ 5V Pulled-up	4.9	—	—	V
	V_{FOL}	V_{SC}=1V, I_{FO}=1mA	—	—	0.95	V

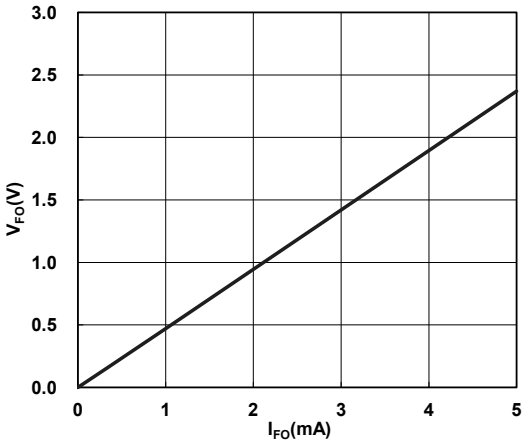


Fig.3-1-7 Fo terminal typical V-I characteristics (V_D=15V, T_j=25°C)

3.1.5 Snubber circuit

During switching, high voltage is induced in power circuit stray inductance by the high di/dt of the main current when the stray inductance is large. This voltage can cause IGBT or diode destruction. In order to avoid this problem, guidelines that should be followed in designing the circuit layout are:

(1) Reduce the L_1 inductance by bringing the connection of the smoothing capacitor close to that of the module and arranging the return connection in a laminated plate structure to cancel the magnetic field.
(2) Connect the snubber capacitor close to the module terminal in order to bypass the high frequency current and absorb the surge voltage.
(3) The smoothing capacitor itself should be of low impedance type.

It is a general measure to suppress the wiring inductance (L_1) of the main circuit as much as possible by (1) or (3), and still suppress surge voltage using (2) when the surge voltage is large. Regarding (2), if the wiring inductance (L_1) is large, the voltage oscillation may increase due to the resonance between Cs and L_1. At that time, oscillation can be suppressed by changing the value of Cs.

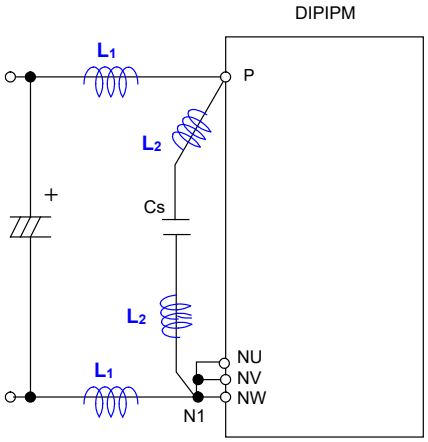


Fig.3-1-8 Recommended snubber circuit location

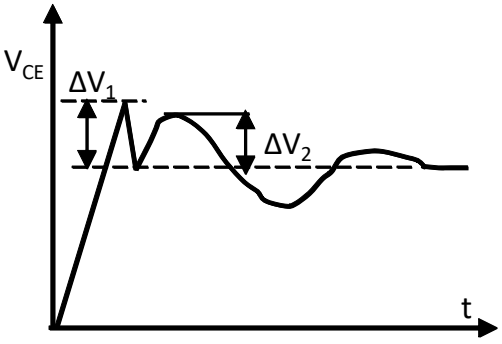


Fig.3-1-9 Waveform example of V_{CE} in turn-off

L_1 : Inductance of the wiring connecting the smoothing capacitor and the DIPIPM.
L_2 : Inductance of the snubber capacitor lead wire. If this inductance is large, it will not be an effective bypass.

In order to prevent DIPIPM from the surge destruction, the wiring length between the smoothing capacitor and DIPIPM P-N terminals should be as short as possible. If the surge voltage is still large, a snubber circuit is recommended. Also, a 1μF or more snubber capacitor should be mounted to the position between P and the connect point of NU, NV and NW terminals as close as possible. Please use a snubber capacitor withstand voltage greater than the device withstand voltage.

A waveform example of collector-emitter voltage V_{CE} in turn-off is shown in Fig.3-1-9. Here the total inductance L is defined as $2\times L_1+2\times L_2$. The formulas for calculating the ΔV_1, ΔV_2, and snubber capacitor Cs design values in the application example of the snubber circuit are shown below.

$$\Delta V_1 = 2 \times L_2 \times \frac{di}{dt} \quad 、 \quad \Delta V_2 = \sqrt{\frac{L \times {I_{OFF}}^2}{Cs}}$$

$$\frac{1}{2} \times \mathrm{L} \times {I_{OFF}}^2 = \frac{1}{2} \times Cs \times {\Delta V_2}^2 \quad 、 \quad Cs = \frac{L \times {I_{OFF}}^2}{{\Delta V_2}^2}$$

In the circuit of Fig. 3-1-8, at first, a surge voltage ($\Delta V_1=2\times L_2\times di/dt$) is generated by di/dt due to turning off the IGBT and wiring inductance (L_2) of the snubber capacitor (Cs). In order to suppress ΔV_1, it is necessary to reduce the snubber wiring inductance L_2.

Next, when L_1 is sufficiently large, resonance occurs between L_1+L_2 and the snubber capacitor (Cs), and its peak voltage ΔV_2 appears. In order to suppress ΔV_2, it is necessary to increase the value of snubber capacitor Cs and to reduce total inductance L. Also, I_{OFF} assumes the current flowing during short-circuit, please calculate as about 10 times rated current.

3.1.6 Influence of Wiring

Influence of pattern wiring around the sense resistor for SC protection and GND is shown below.

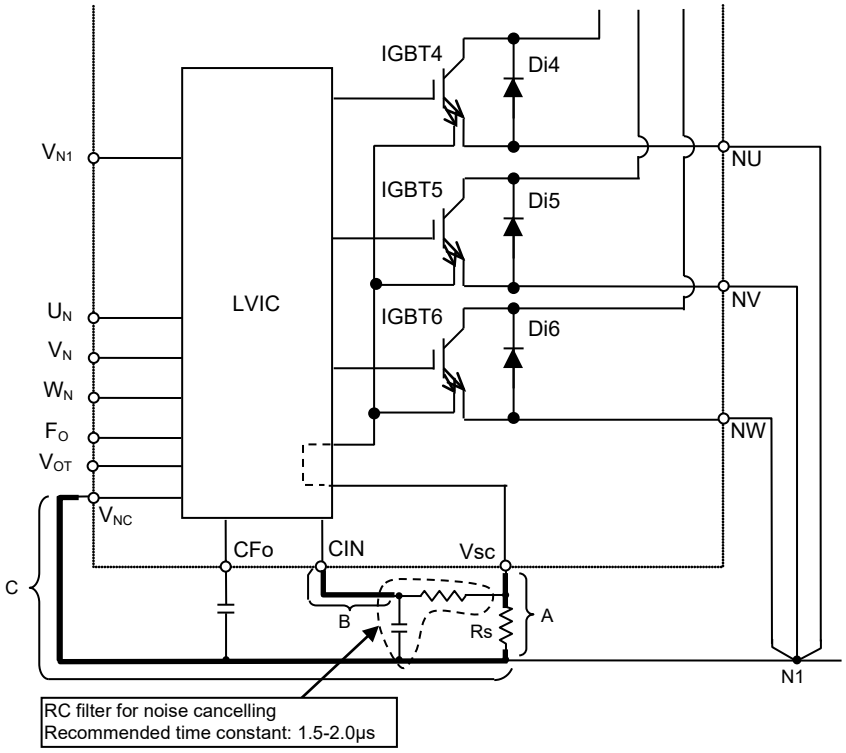


Fig.3-1-10 External protection circuit

(1) Influence of the part-A wiring

The part-A wiring affects SC protection level. SC protection works by judging the voltage of the CIN terminals. If part-A wiring is too long, extra surge voltage generated by the wiring inductance will lead to fluctuation of SC protection level. This wiring should be as short as possible for limiting the surge voltage.

(2) Influence of the part-B wiring pattern

RC filter is added to remove noise influence occurring on the sense resistor. Filter effect will dropdown and noise will easily superimpose on the wiring, if part-B wiring (=after filtering part) is too long. Please install the RC filter near CIN, V_{NC} terminals as close as possible.

(3) Influence of the part-C wiring pattern

Part-C wiring pattern gives influence to all the items described above, maximally shorten the GND wiring is expected. If control GND is connected to power GND by broad pattern, it may cause malfunction by power GND fluctuation. It is recommended to connect control GND and power GND at only a point at which NU, NV, NW are connected to power GND line.

3.1.7 Precaution for Wiring on PCB

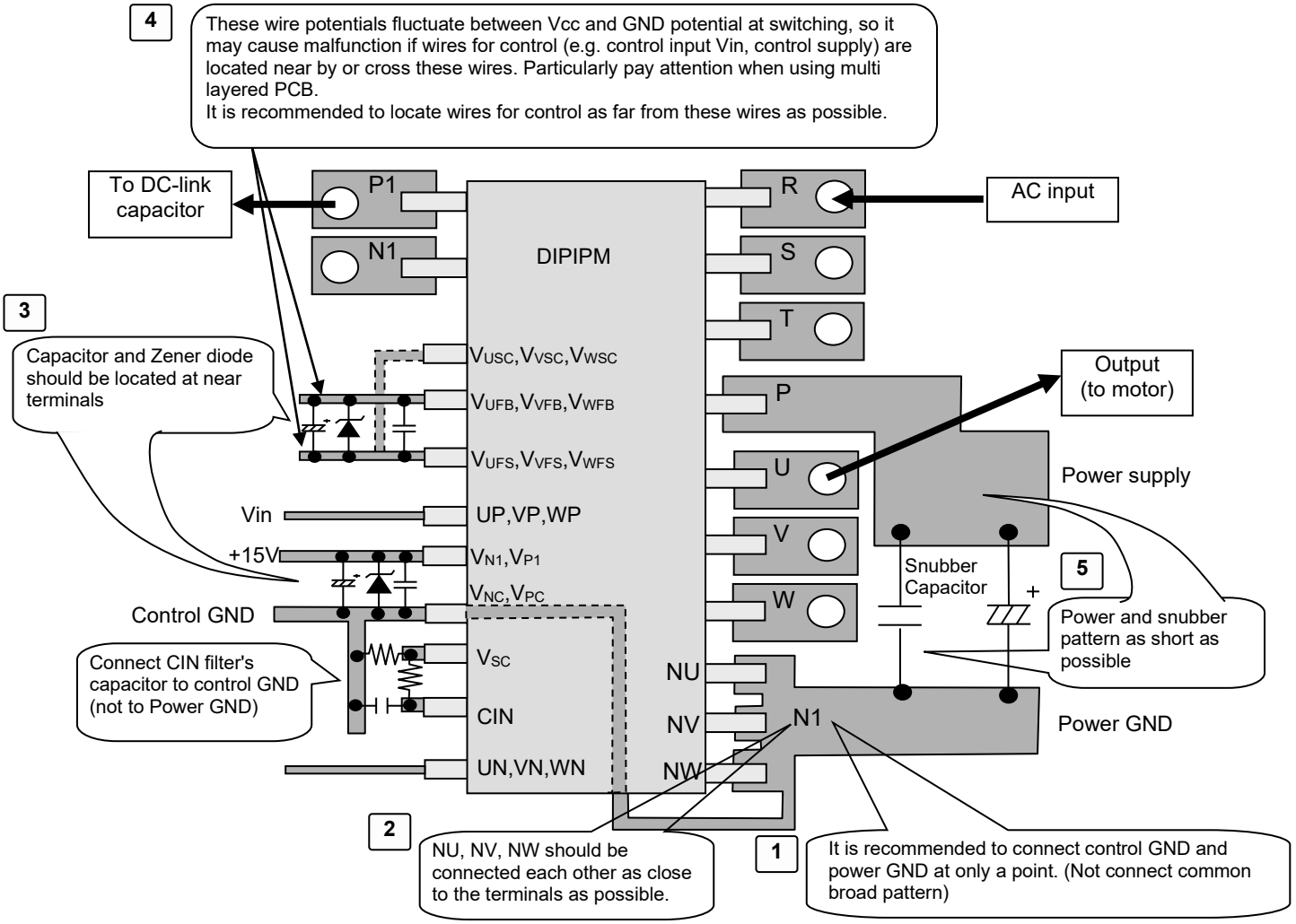


Fig.3-1-11 Precaution for wiring on PCB

The case example of trouble due to PCB pattern

	Case example	Matter of trouble
1	Control GND pattern overlaps power GND pattern.	The surge, generated by the wiring pattern and di/dt of noncontiguous big current flows to power GND, transfers to control GND pattern. it causes the control GND level fluctuation, so that the input signal based on the control GND fluctuates too. Finally the arm short occurs.
	Ground loop pattern exists.	Stray current flows to GND loop pattern, so that the control GND level and input signal level (based on the GND) fluctuates. Then the arm short occurs.
2	Long pattern between NU, NV, NW terminals and N1	Long wiring pattern has big parasitic inductance and generates high surge when switching. This surge causes the matter as below. •HVIC malfunction due to VS voltage (output terminal potential) dropping excessively. •LVIC surge destruction
3	Capacitors or zener diodes are nothing or located far from the terminals.	IC surge destruction or malfunction occurs.
4	The input lines are located parallel and close to the floating supply lines for P-side drive.	Cross talk noise might be transferred through the capacitance between these floating supply lines and input lines to DIPIPM. Then incorrect signals are input to DIPIPM input, and arm short (short circuit) might occur.
5	Long P pattern and power GND pattern	Long wiring pattern has big parasitic inductance and generates high surge when switching. This surge causes the matter as below. •HVIC malfunction due to VS voltage (output terminal potential) dropping excessively. •LVIC surge destruction
	Long snubber circuit pattern	Power chip surge destruction

3.1.8 SOA of Large DIPIPM+ at switching state

The SOA (Safety Operating Area) of Large DIPIPM+ series are described as follows;

V_{CES} : Maximum rating of IGBT collector-emitter voltage

V_{CC} : DC-link voltage applied on P-N terminals

$V_{CC(surge)}$: Voltage between P and N terminals including surge voltage which will be generated due to wiring inductance between DIPIPM and DC-link capacitor at switching state.

$V_{CC(PROT)}$: Maximum DC-link voltage in which DIPIPM can protect itself when short circuit happens.

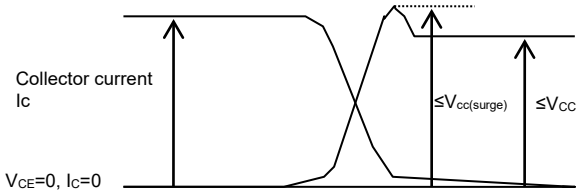


Fig.3-1-12 SOA at switching mode

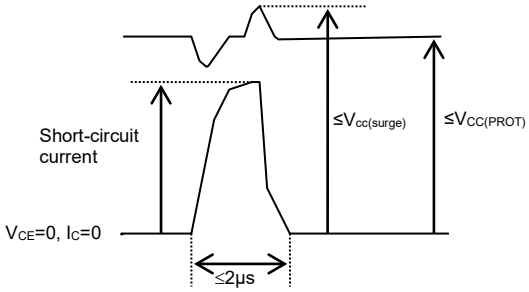


Fig.3-1-13 SOA at short-circuit mode

In case of switching

V_{CES} is the maximum voltage rating of IGBTs for 1200V as withstanding voltage. $V_{CC(surge)}$ is specified to maximum 1000V subtracted 200V or less of surge voltage by internal wiring inductance of Large DIPIPM+ from V_{CES}. Furthermore, also V_{CC} is specified to maximum 800V because it should be considered about surge voltage by wiring inductance between Large DIPIPM+ terminals and DC-link capacitor, then the maximum Vcc is subtracted 200V from $V_{CC(surge)}$ as the margin.

In case of short-circuit

V_{CES} and V_{CC}(surge) are same definition as the case of switching. Vcc is specified to 800V because it should be considered about larger surge voltage by wiring inductance at the turning off short-circuit current, then maximum Vcc is subtracted 200V from $V_{CC(surge)}$ as the margin.

3.1.9 SCSOA

Fig.3-1-14~17 show the typical SCSOA performance curves of each products.

The measurement condition is described as follows;
V_{CC}=800V, Tj=150°C at initial state, $V_{CC(surge)}$≦1000V(surge included), non-repetitive,2m load.

Please refer Fig.3-1-15 for PSS50NE1CT(50A/1200V), for instance. It shows Large DIPIPM+ can safely shut down an SC current which is about 10 times of its current rating under above conditions, when the IGBT shuts off by 4.8μs at V_D=16.5V. Since the SCSOA (Short Circuit Safety Operating Area) will vary with the control supply voltage, DC-link voltage, and so on, it is necessary to set time constant of RC filter with a margin.

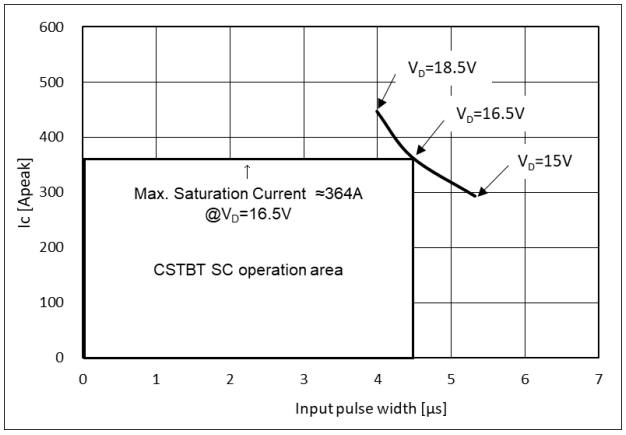


Fig.3-1-14 Typical SCSOA curve of PSS35NE1CT

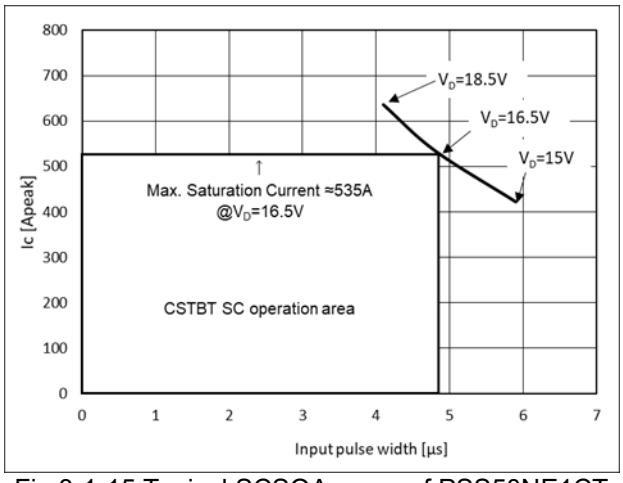


Fig.3-1-15 Typical SCSOA curve of PSS50NE1CT

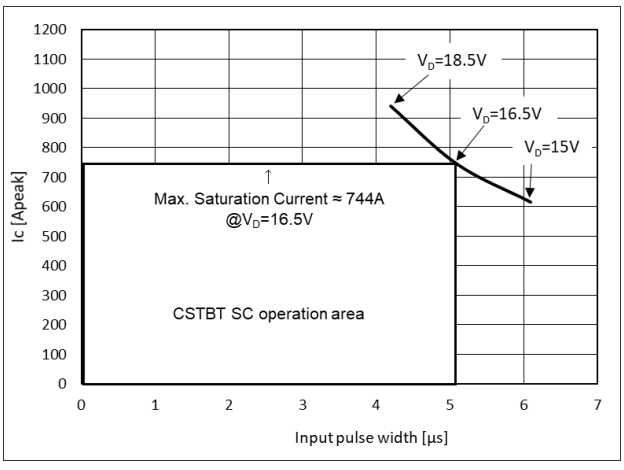


Fig.3-1-16 Typical SCSOA curve of PSS75NE1CT

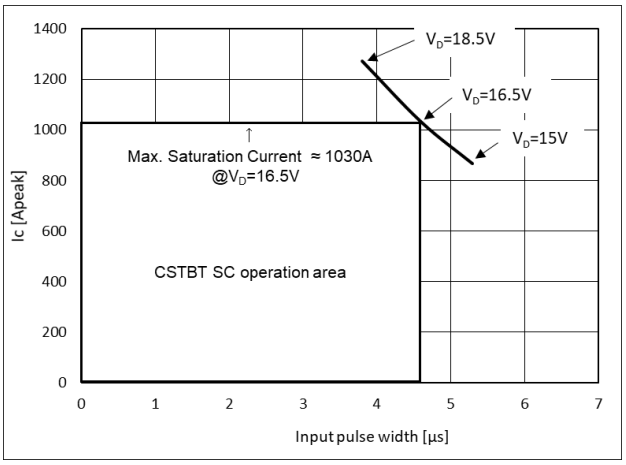


Fig.3-1-17 Typical SCSOA curve of PSS100NE1CT

3.1.10 Power Life Cycles

When DIPIPM is in operation, repetitive temperature variation will happen on the IGBT junctions (ΔTj). The amplitude and the times of the junction temperature variation affect the device lifetime.

Fig.3-1-17 shows the IGBT power cycle curve as a function of average junction temperature variation (ΔTj). (The curve is a regression curve based on 3 points of ΔTj=46, 88, 98K with regarding to failure rate of 0.1%, 1% and 10%. These data are obtained from the reliability test of intermittent conducting operation)

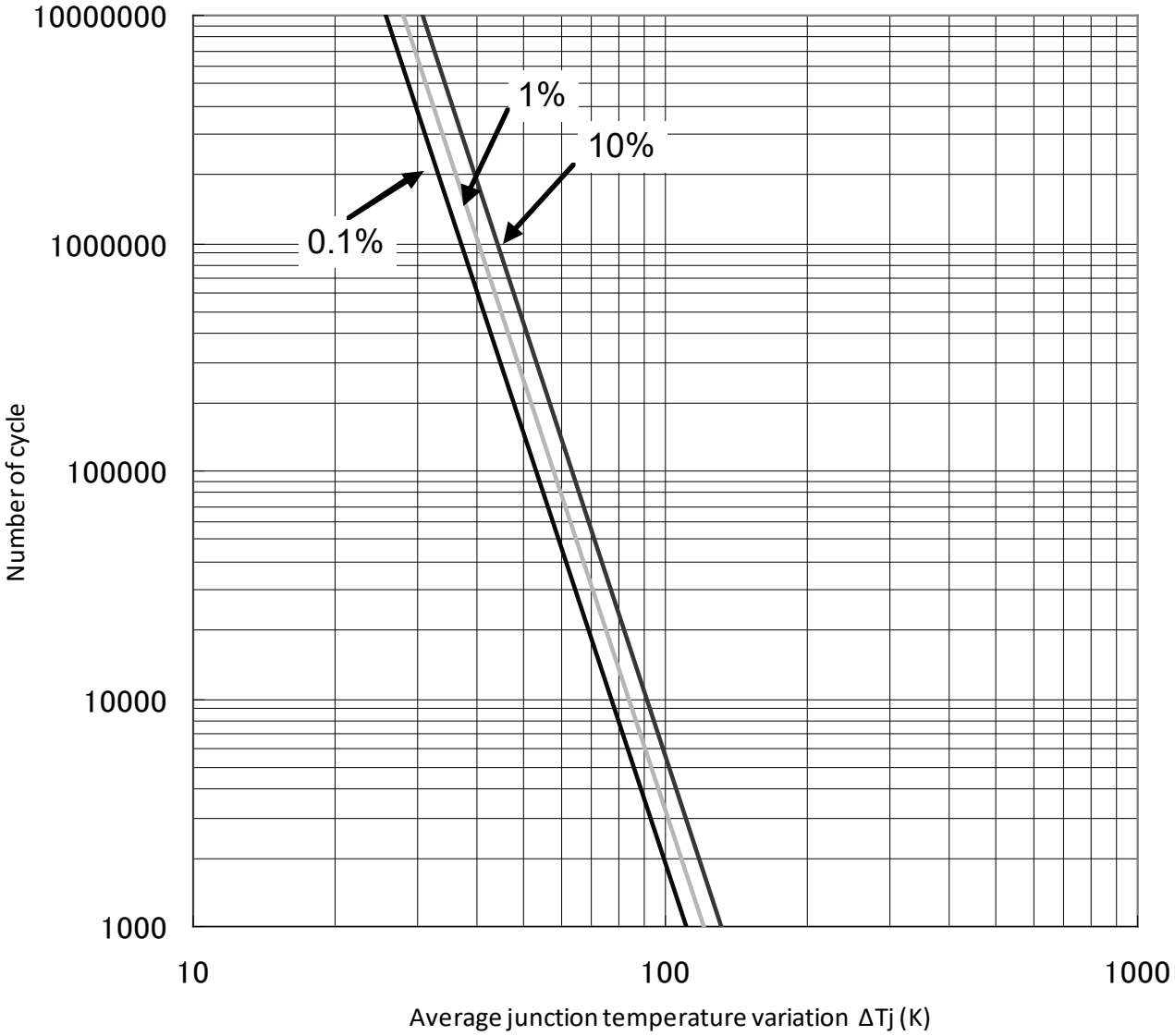


Fig.3-1-17 Power cycle curve

3.2 Power loss and thermal dissipation calculation

3.2.1 Power loss calculation

Simple expressions for calculating average power loss are given as follows;

● Scope

The power loss calculation intends to provide users a way of selecting a matched power device for their VVVF inverter application. However, it is not expected to use for limit thermal dissipation design.

● Assumptions

(1) PWM controlled VVVF inverter with sinusoidal output;
(2) PWM signals are generated by the comparison of sine waveform and triangular waveform.
(3) Duty amplitude of PWM signals varies between $\frac{1-D}{2} \sim \frac{1+D}{2}$ (%/100), (D: modulation depth).
(4) Output current various with Icp·sinx and it does not include ripple.
(5) Power factor of load output current is cosθ, ideal inductive load is used for switching.

● Expressions Derivation

PWM signal duty is a function of phase angle x as $\frac{1+\mathrm{D}\times\sin\mathrm{x}}{2}$ which is equivalent to the output voltage variation. From the power factor cosθ, the output current and its corresponding PWM duty at any phase angle x can be obtained as below:

$$Output\ \ current = Icp \times \sin x$$

$$PWM\ \ \ Duty = \frac{1 + D \times \sin(x + \theta)}{2}$$

Then, $V_{CE(sat)}$ and V_{EC} at the phase x can be calculated by using a linear approximation:

$$Vce(sat) = Vce(sat)(@\, Icp \times \sin x)$$
$$Vec = (-1) \times Vec(@\, Iecp(= Icp) \times \sin x)$$

Thus, the static loss of IGBT is given by:

$$\frac{1}{2\pi}\int_0^{\pi} (Icp \times \sin x) \times Vce(sat)(@\, Icp \times \sin x) \times \frac{1 + D\sin(x + \theta)}{2} \bullet dx$$

Similarly, the static loss of free-wheeling diode is given by:

$$\frac{1}{2\pi}\int_{\pi}^{2\pi} ((-1) \times Icp \times \sin x)((-1) \times Vec(@\, Icp \times \sin x) \times \frac{1 + D\sin(x + \theta)}{2} \bullet dx$$

On the other hand, the dynamic loss of IGBT, which does not depend on PWM duty, is given by:

$$\frac{1}{2\pi}\int_0^{\pi} (Psw(on)(@\, Icp \times \sin x) + Psw(off)(@\, Icp \times \sin x)) \times fc \bullet dx$$

FWDi recovery characteristics can be approximated by the ideal curve shown in Fig.3-2-1, and its dynamic loss can be calculated by the following expression:

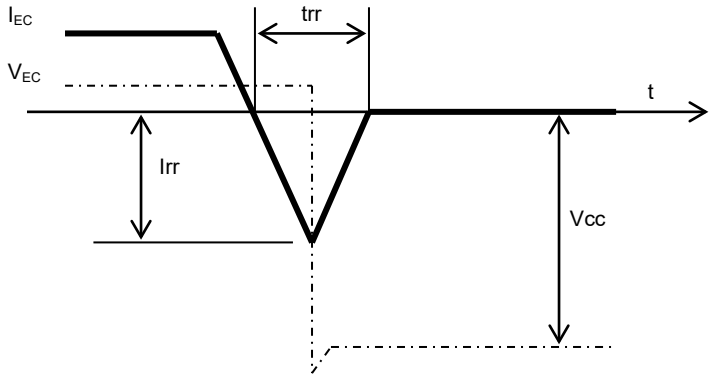


Fig.3-2-1 Ideal FWDi recovery characteristics curve

$$Psw = \frac{Irr \times Vcc \times trr}{4}$$

Recovery occurs only in the half cycle of the output current, thus the dynamic loss is calculated by:

$$\frac{1}{2}\int_{\pi}^{2\pi} \frac{Irr(@\,Icp \times \sin x) \times Vcc \times trr(@\,Icp \times \sin x)}{4} \times fc \bullet dx$$
$$= \frac{1}{8}\int_{\rho}^{2\pi} Irr(@\,Icp \times \sin x) \times Vcc \times trr(@\,Icp \times \sin x) \times fc \bullet dx$$

- Attention of applying the power loss simulation for inverter designs
  - Divide the output current period into fine-steps and calculate the losses at each step based on the actual values of PWM duty, output current, $V_{CE(sat)}$, V_{EC}, and Psw corresponding to the output current. The worst condition is most important.
  - PWM duty depends on the signal generating way.
  - The relationship between output current waveform or output current and PWM duty changes with the way of signal generating, load, and other various factors. Thus, calculation should be carried out on the basis of actual waveform data.
  - $V_{CE(sat)}$,V_{EC} and Psw(on, off) should be the values at T_j=125°C.

3.2.2 Large DIPIPM+ performance according to carrier frequency

Fig.3-2-2 shows the typical characteristics of allowable effective current vs. carrier frequency under the following inverter operating conditions based on power loss simulation results for Large DIPIPM+ series.

Conditions: V_{CC}=600V, V_D=V_{DB}=15V, $V_{CE(sat)}$=Typ., P.F=0.8, Switching loss=Typ., Tj=125°C, Tc=100°C, Rth(j-c)=Max., 3-phase PWM modulation, 60Hz sine waveform output

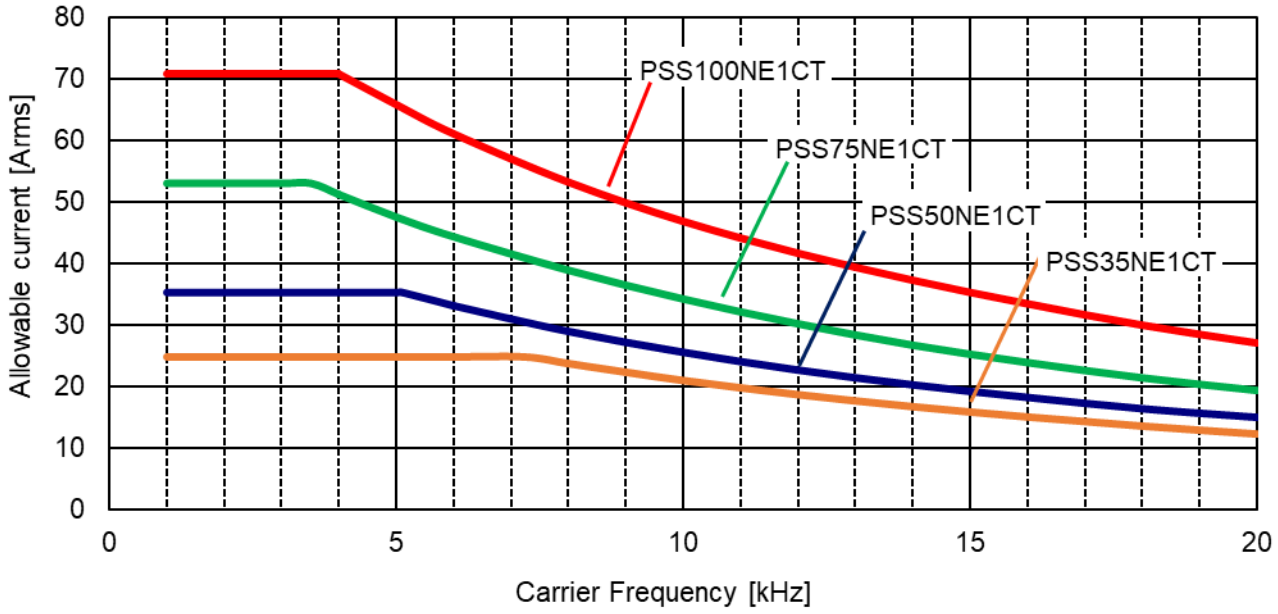


Fig.3-2-2 Effective current-carrier frequency characteristics

Fig.3-2-2 shows one of the example of estimating allowable inverter output effective current with different carrier frequency and allowable maximum operating temperature condition (T_c=100°C. T_j=125°C). The results may change for different control strategy and motor types. Anyway please ensure that there is no large current over device rating flowing continuously.

The inverter loss can be calculated by the free power loss simulation software which is uploaded on the web site.
URL: http://www.MitsubishiElectric.com/semiconductors/

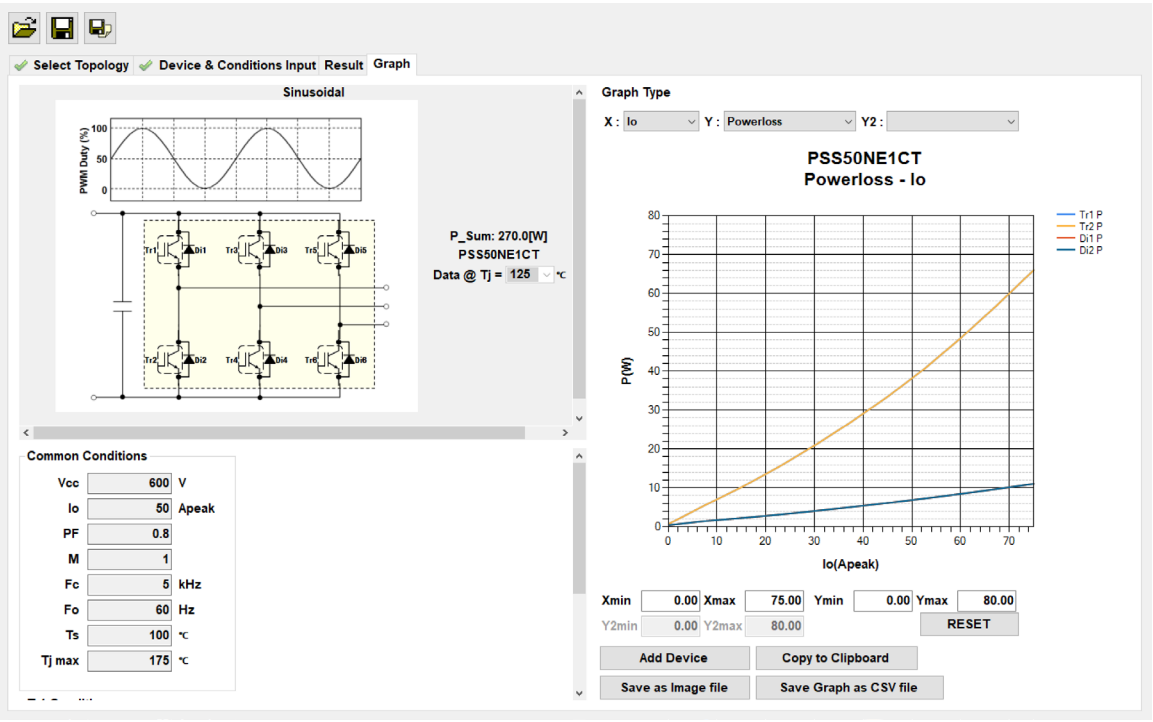


Fig.3-2-3 Loss simulator screen image

3.3 Noise and ESD withstand capability

3.3.1 Evaluation circuit of noise withstand capability

Large DIPIPM+ series have been confirmed to be with over +/-2.0kV noise withstand capability by the noise evaluation under the conditions shown in Fig.3-3-1. However noise withstand capability greatly depends on the test environment, the wiring patterns of control substrate, parts layout and other factors, it is recommended to conduct enough evaluation using prototype product.

[Condition]
V_{CC}=600V, V_D=15V, T_a=25°C, no load

Scheme of applying noise: From AC line (R, S, T), Period T=16ms, Pulse width tw=0.05-1μs, input in random.

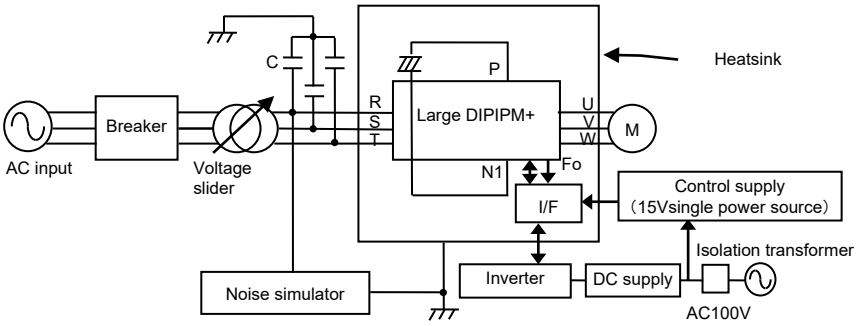


Fig.3-3-1 Noise withstand capability evaluation circuit

(note)
C1: AC line common-mode filter 4700pF, PWM signals are input from microcomputer by using opto-couplers, 15V single power supply, Test is performed with IM

3.3.2 Countermeasures and precautions

Large DIPIPM+ series are improved of noise withstand capabilities by means of reducing parts quantity, lowering internal wiring parasitic inductance, and reducing leakage current. But when the noise affects on the control terminals of DIPIPM (due to wiring pattern on PCB), the short circuit or malfunction of SC protection may occur. In that case, below countermeasures are recommended.

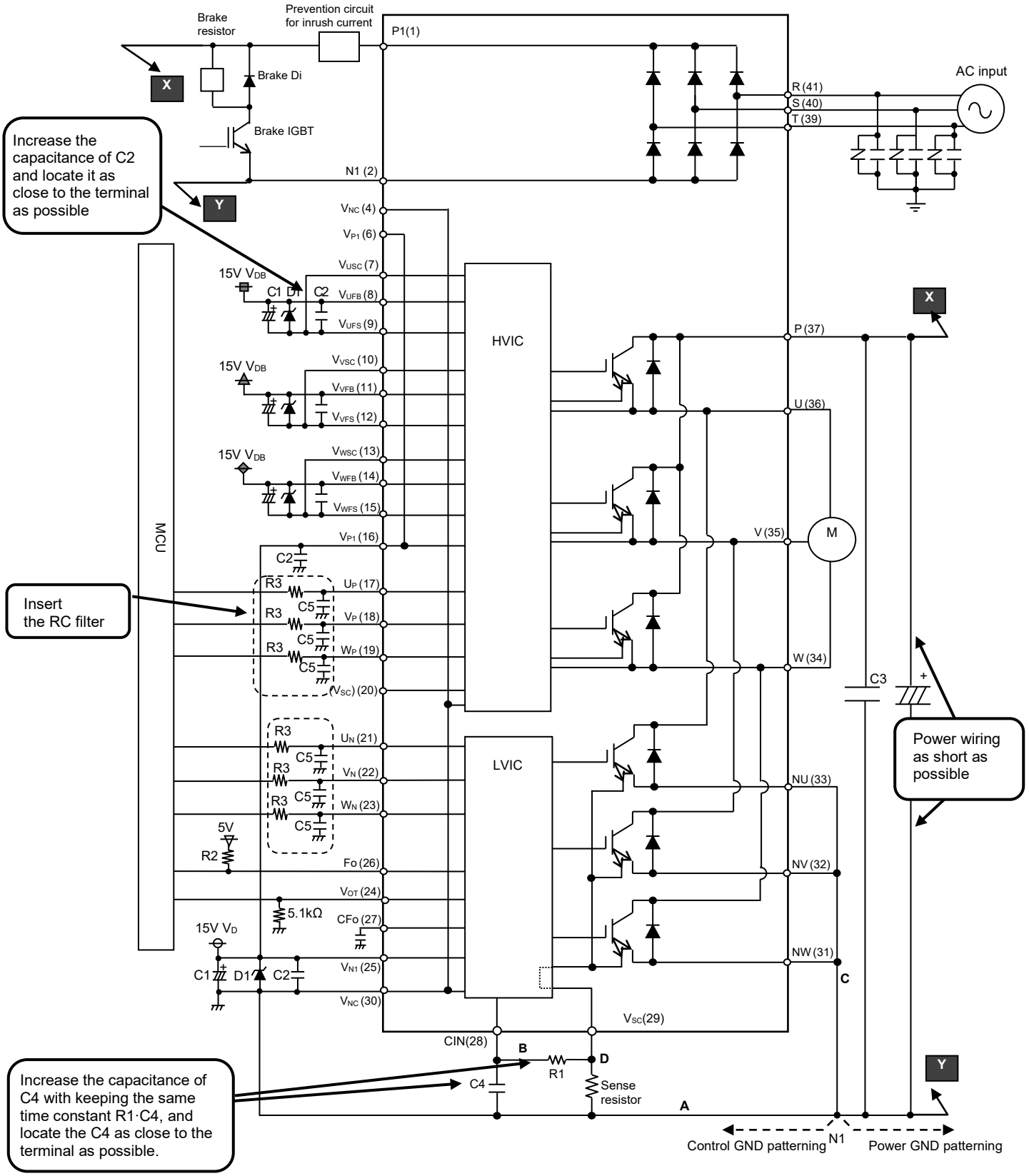


Fig.3-3-2 Example of countermeasures for inverter part

3.3.3 Static electricity withstand capability

DIPIPM has been confirmed to be with typical +/-1kV or more withstand capability against static electricity from the following tests shown in Fig.3-3-3, 4. HBM method: C=100pF, R=1.5 kΩ.

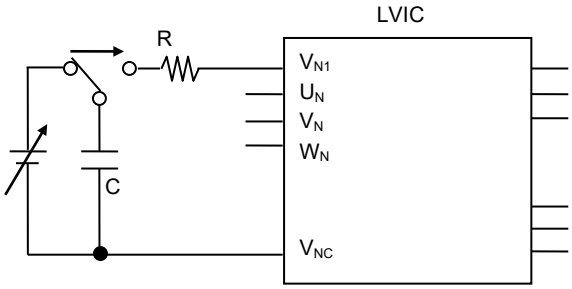


Fig.3-3-3 Surge test circuit example (V_{N1} terminal)

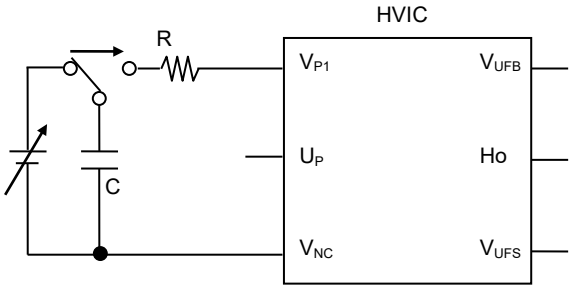


Fig.3-3-4 Surge test circuit example (V_{P1} terminal)

CHAPTER 4 : Bootstrap Circuit Operation

4.1 Bootstrap Circuit Operation

For three phase inverter circuit driving, it requires four isolated control supplies for driving three P-side ICs and one N-side IC. But using floating control supply with bootstrap circuit can reduce the number of isolated control supplies from four to one, it requires N-side control supply only.

Bootstrap circuit consists of a bootstrap diode(BSD), a bootstrap capacitor(BSC) and a current limiting resistor. DIPIPM+ series integrates BSD and limiting resistor, so it can make bootstrap circuit by adding outer BSC only. The BSC works as a control supply for driving P-side IGBT. The BSC supplies gate charge when P-side IGBT turning ON and circuit current of logic circuit on P-side driving IC. (Fig.4-1-2) Since a capacitor is used as substitute for isolated supply, its supply capability is limited. This floating supply driving with bootstrap circuit is suitable for small supply current products like DIPIPM.

Charge consumed by driving circuit is re-charged from N-side 15V control supply to BSC via current limiting resistor and BSD when voltage of output terminal (U, V or W) goes down to GND potential in inverter operation. The BSC cannot be charged enough depending on its switching condition, BSC capacitance and so on. Deficient charge leads to too low voltage of BSC and might work “under voltage protection” (UV). This situation makes the loss of P-side IGBT increase by low gate voltage or stop switching. So it is necessary to consider and evaluate enough for designing bootstrap circuit. For more detail information about driving by the bootstrap circuit, refer the DIPIPM application note "Bootstrap Circuit Design Manual"

The BSD characteristics for DIPIPM+ series and the circuit current characteristics in switching situation of P-side IGBT are described as follows.

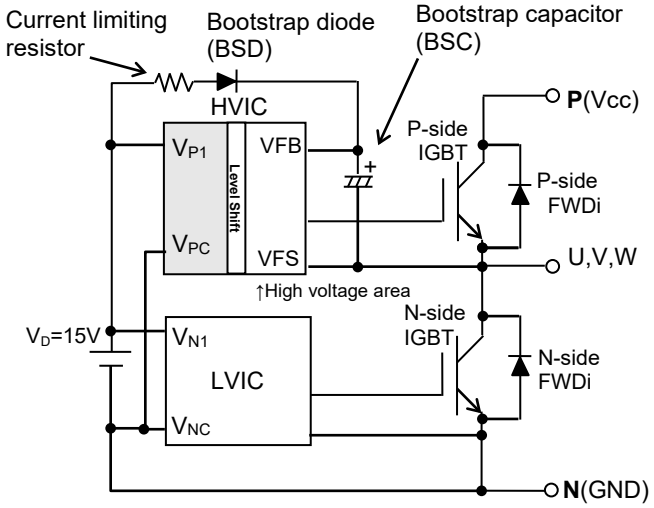


Fig.4-1-1 Bootstrap Circuit Diagram

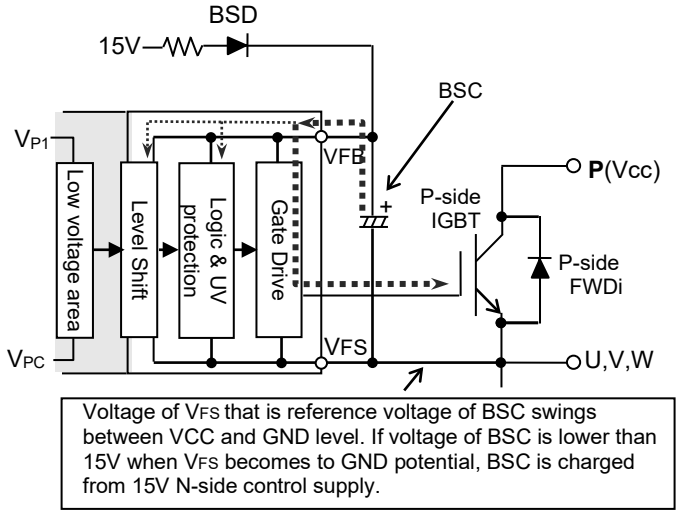


Fig.4-1-2 Bootstrap Circuit Diagram

4.2 Bootstrap supply circuit current at switching state

Bootstrap supply circuit current I_{DB} at steady state is 2.4mA maximum. At switching state, the circuit current exceeds 2.4mA and increases proportional to carrier frequency, because gate charge and discharge are repeated at each switching state. Fig.4-2-1~4 show typical I_{DB} vs. carrier frequency fc characteristics for Large DIPIPM+ series.

[Condition]

V_{CC}=800V, V_D=V_{DB}=15V, Tj=150°C

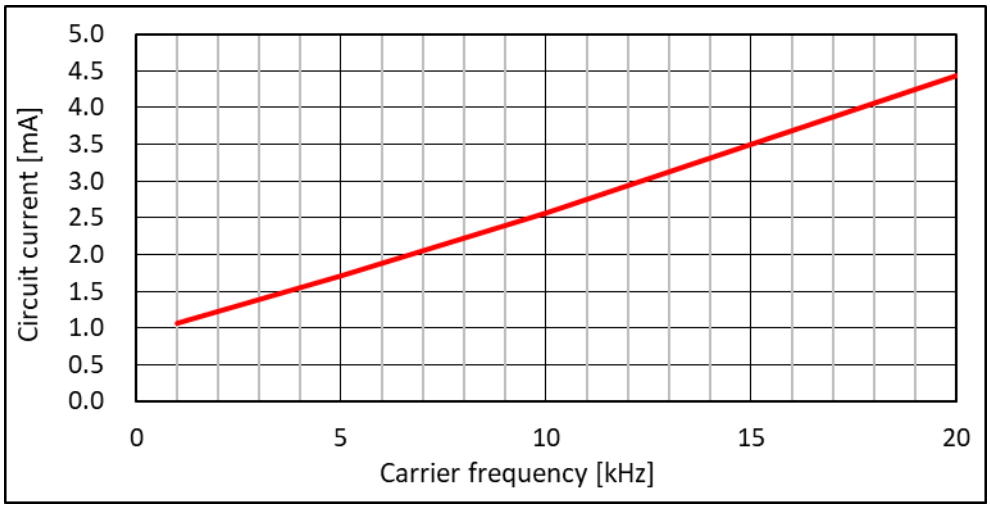


Fig. 4-2-1. I_{DB} vs. Carrier frequency for PSS35NE1CT

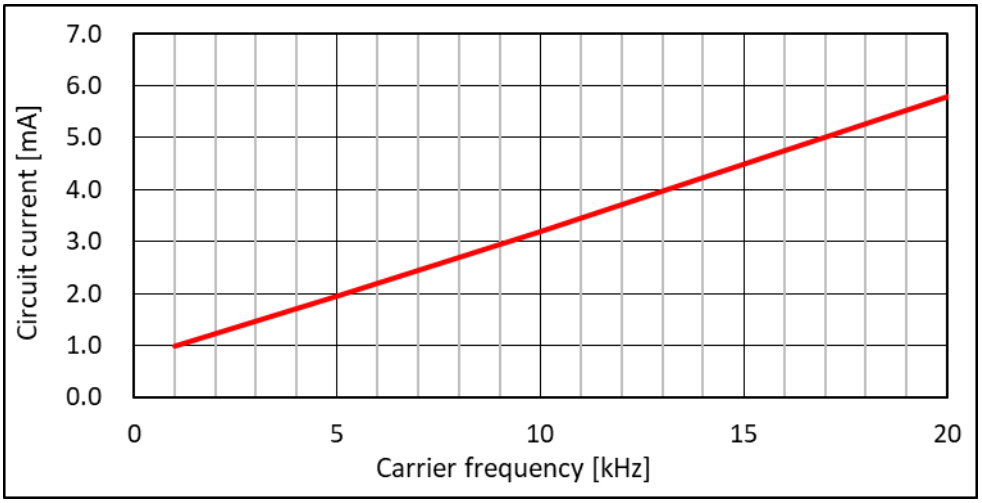


Fig. 4-2-2. I_{DB} vs. Carrier frequency for PSS50NE1CT

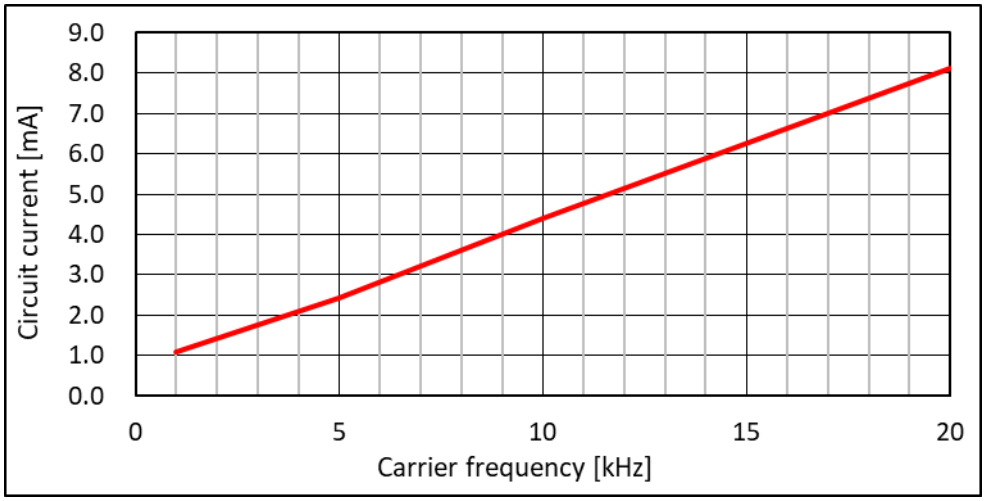


Fig. 4-2-3. I_{DB} vs. Carrier frequency for PSS75NE1CT

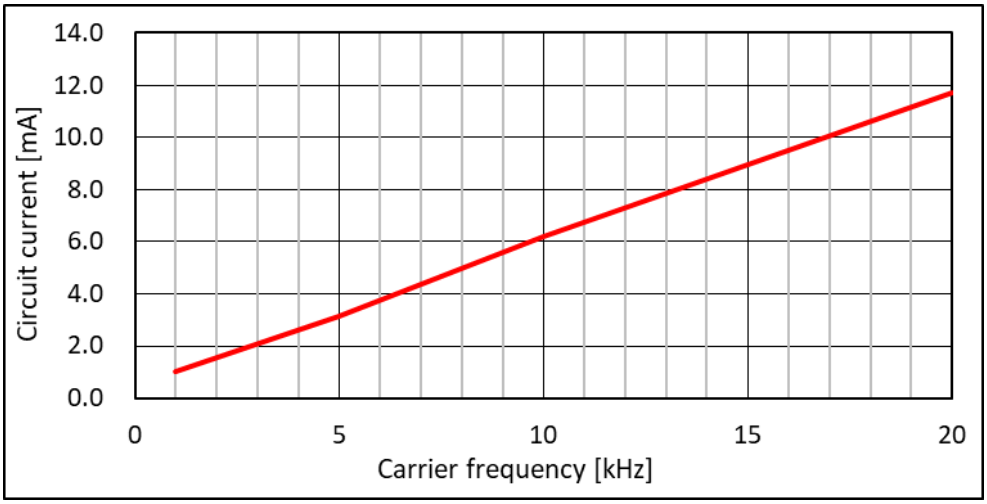


Fig. 4-2-4. I_{DB} vs. Carrier frequency for PSS100NE1CT

4.3 Note for designing the bootstrap circuit

When each device for bootstrap circuit is designed, it is necessary to consider various conditions such as temperature characteristics, change by lifetime, variation and so on. Note for designing these devices are listed as below. For more detail information about driving by the bootstrap circuit, refer the DIPIPM application note "Bootstrap Circuit Design Manual"

(1) Bootstrap capacitor

BSC employs electrolytic capacitors in general, and recently ceramic capacitor with large capacitance is also applied to it. Please note that DC bias characteristic is considerably different between electrolytic capacitor and of ceramic capacitor when applying DC voltage. Its characteristics especially differ with large capacitance type. Table 4-3-1 shows example of difference between the above two capacitors.

Table 4-3-1 Differences of capacitance characteristics between electrolytic and ceramic capacitors

	Electrolytic capacitor	Ceramic capacitor (large capacitance type)
Temperature characteristics (Ta:-20~ 85°C)	•Aluminum type: Low temp.: -10% High temp: +10% •Conductive polymer aluminum solid type: Low temp.: -5% High temp: +10%	Different due to temp. characteristics rank Low temp.: -5%~0% High temp.: -5%~-10% (in the case of B,X5R,X7R ranks)
DC bias characteristics (Applying DC15V)	Nothing within rating voltage	Different due to temp. characteristics, rating voltage, package size and so on -70%~-15%

DC bias characteristic of electrolytic capacitor is no problem, however, it is necessary to note its ripple capability by repetitive charge and discharge, its ambient temperature which affects the capacitor's life time greatly, and so on. These above characteristics are just example data which are quoted from the WEB site, so it is recommended to inquiry to the capacitor manufacturers about detailed characteristics.

(2) Bootstrap diode

It is recommended for BSD to have same or higher blocking voltage with collector-emitter voltage V_{CES} of IGBT in DIPIPM. (i.e. 1200V or more is needed in the case of Large DIPIPM+.) And its recovery time trr should be less than 100ns. (Fast recovery type)

Also **it is highly recommended to apply the high quality product such as small variations of blocking voltage.** If BSD broke by impressed overvoltage and shorted, it leads to the control ICs over voltage destruction because DC-link voltage (Vcc) is impressed upon low voltage area of control ICs. Then DIPIPM will lose various functions like protection and gate driving and it may lead to serious system destruction.

(3) Current limiting resistor

When designing limiting resistor, it is important to note its power rating, surge withstand capability (there is the possibility that surge may be impressed on the resistor when switching ON or OFF timing) and so on.
Especially if small chip type resistor is applied, it is recommended to select anti-surge designed type. For detailed information, please refer to the resistor manufacturer.

4.4 Initial charging in bootstrap circuit

In case of applying bootstrap circuit, it is necessary to charge to the BSC initially because voltage of BSC is 0V at initial state or it may drop down to the trip level of under voltage protection after long suspending period (even 1s). BSC charging is performed by turning on all N-side IGBT normally. When outer load (e.g. motor) is connected to the DIPIPM, BSC charging may be performed by turning on only one phase N-side IGBT since potential of all output terminals will go down to GND level through the wiring in the motor. But its charging efficiency might become lower due to some cause. (e.g. wiring resistance of motor)

There are mainly two procedures for BSC charging. One is performed by one long pulse, and another is conducted by multiple short pulses. Multi pulse method is used when there are some restriction like control supply capability and etc.

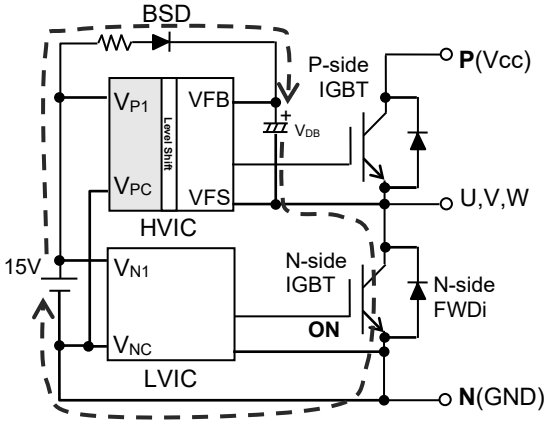


Fig.4-4-1 Initial charging root

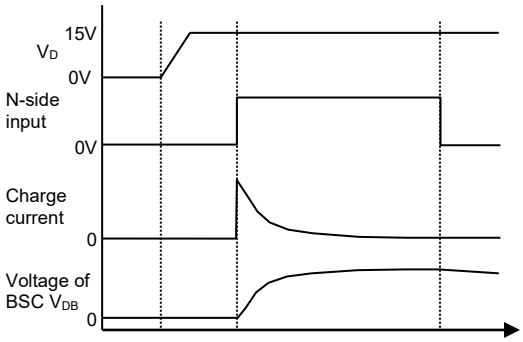


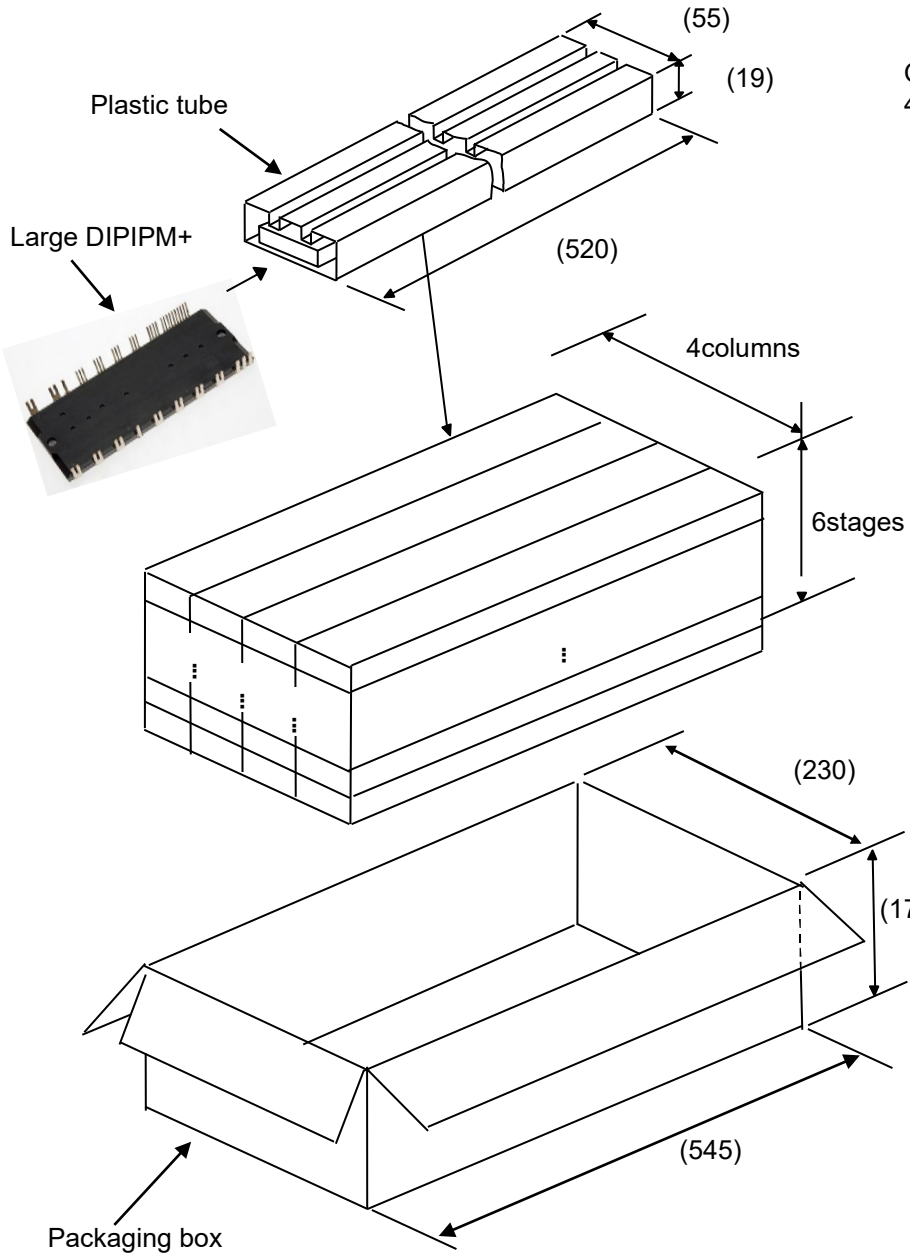
Fig .4-4-2 Example of waveform by one charging pulse

Initial charging needs to be performed until voltage of BSC exceeds 13V, recommended minimum supply voltage. (It is recommended to charge higher than 13V with consideration for voltage drop from the end of charging to start time of inverter operation.)

After BSC was charged, it is recommended to input one ON pulse to the P-side input for reset of internal IC state before starting system. Input pulse width is needed to be longer than allowable minimum input pulse width PWIN(on). (3.0μs or more for Large DIPIPM+. Please refer the datasheet for each product in detail.)

CHAPTER 5 : PACKAGE HANDLING

5.1 Packaging Specification



Quantity:
4 pieces / 1 tube

Total amount in one box (max):
Tube Quantity: 4 × 6=24pcs
IPM Quantity(max.):
4 × 24 ＝96pices

When it isn't fully filled by tubes at top stage, cardboard spacers or empty tubes are inserted for filling the spcae of top stage.

Mass:
About 90g / Large DIPIPM+
About 500g / tube
About 13kg / box

Spacers are put on the top and bottom of the box. If there is some space on top of the box, additional buffer materials are also inserted.

Fig.5-1 Packaging Specification

5.2 Handling Precautions

⚠ Cautions	
Transportation	・Put package boxes in the correct direction. Putting them upside down, leaning them or giving them uneven stress might cause electrode terminals to be deformed or resin case to be damaged. ・Throwing or dropping the packaging boxes might cause the devices to be damaged. ・Wetting the packaging boxes might cause the breakdown of devices when operating. Pay attention not to wet them when transporting on a rainy or a snowy day.
Storage	・We recommend temperature and humidity in the ranges 5-35°C and 45-75%, respectively, for the storage of modules. The quality or reliability of the modules might decline if the storage conditions are much different from the above.
Long storage	・When storing modules for a long time (more than one year), keep them dry. Also, when using them after long storage, make sure that there is no visible flaw, stain or rust, etc. on their exterior.
Surroundings	・Keep modules away from places where water(including dew condensation) or organic solvent may attach to them directly or where corrosive gas, explosive gas, fine dust or salt, etc. may exist. They might cause serious problems.
Flame resistance	・The epoxy resin of case material is flame-resistant type (UL standard 94V-0), but they are not noninflammable.
Anti-electrostatic Measures	・ICs and power chips with MOS gate structure are used for the DIPIPM power modules. Please keep the following notices to prevent modules from being damaged by static electricity. (1) Precautions against the device destruction caused by the ESD When the ESD of human bodies, packaging and etc. are applied to terminal, it may damage and destroy devices. The basis of anti-electrostatic is to inhibit generating static electricity possibly and quick dissipation of the charged electricity. *Containers that charge static electricity easily should not be used for transit and for storage. *Terminals should be always shorted with a carbon cloth or the like until just before using the module. Never touch terminals with bare hands. *Should not be taking out DIPIPM from tubes until just before using DIPIPM and never touch terminals with bare hands. *During assembly and after taking out DIPIPM from tubes, always earth the equipment and your body. It is recommended to cover the work bench and its surrounding floor with earthed conductive mats. *When the terminals are open on the printed circuit board with mounted modules, the modules might be damaged by static electricity on the printed circuit board. *If using a soldering iron, earth its tip. (2)Notice when the control terminals are open *When the control terminals are open, do not apply voltage between the collector and emitter. It might cause malfunction. *Short the terminals before taking a module off.
Anti-overvoltage Measures	・Precautions for overvoltage destruction. It should be noted that overvoltage destruction of DIPIPM might be caused by applying surges to inner chips (power chips and ICs) when surges are impressed to DIPIPM package directly or indirectly via the circuit board by surge discharging due to mis-operation on the in-circuit inspection process (e.g. plug off the connector of test board before discharging its capacitor, imperfect contact of the connector, and so on).

Large DIPIPM+ Series Application note