TECHNICAL BULLETIN

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[Title] Caution for the Universal model QCPU using the SCJ instruction **[Date of Issue]** Dec.,'08
[Relevant Models] Q00UJCPU, Q00UCPU, Q01UCPU, Q02UCPU, Q03UDCPU, Q04UDHCPU, Q06UDHCPU, Q10UDHCPU, Q13UDHCPU, Q20UDHCPU, Q26UDHCPU, Q03UDECPU, Q04UDEHCPU, Q06UDEHCPU, Q10UDEHCPU, Q13UDEHCPU, Q20UDEHCPU, Q26UDEHCPU

Thank you for your continued support of Mitsubishi programmable controllers, MELSEC series.

This bulletin provides a caution when using the Universal model QCPU with the SCJ instruction.

1. Caution

When using the Universal model QCPU with the SCJ instruction, insert the special relay (SM400) (or the NOP instruction) in immediately before the SCJ instruction.
However, if the immediately preceding instruction meets the following conditions, use the existing programs.

2. Condition

- When the instructions listed in Table 1 are executed immediately before the SCJ instruction or subset processing is used for the listed instructions in Table 2 to be executed immediately before the SCJ instruction.

Table 1 Instruction tables

Category	Instructions
Association instructions	ANB, EGF, EGP, INV, MEF, MEP, MPP, MRD, ORB
Select Refresh Instruction	COM
Reset	LEDR
Master control	MC
No operations	NOP, NOPLF
Output	RST, SET
Stop	STOP
Trace Set	TRACE
Trace Reset	TRACER
WDT Reset	WDT, WDTP

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Table 2 Instruction tables (Instructions that subset processing is used)

Category	Instructions
BIN 16-bit addition and subtraction operations	+, +P, -, -P
BIN 16-bit multiplication and division operations	*, *P, /, /P
BIN 32-bit addition and subtraction operations	D+, D+P, D-, D-P
BIN 32-bit multiplication and division operations	D*, D*P, D/, D/P
Addition and subtraction of floating decimal point data(Single precision)	E+, E+P, E-, E-P
Multiplication and division of floating decimal point data(Single precision)	E*, E*P
Contact	AND, ANDF, ANDP, ANI, LD, LDF, LDI, LDP, OR, ORF, ORI, ORP
Output	OUT
BIN 16-bit data comparisons	AND>=, AND<, AND<=, AND<>, AND=, AND>, LD>=, LD<, LD<=, LD<>, LD=, LD>, OR<, OR<=, OR<>, OR=, OR>, OR>=
BIN 32-bit data comparisons	ANDD<, ANDD<=, ANDD<>, ANDD=, ANDD>, ANDD>=, LDD<, LDD<=, LDD<>, LDD=, LDD>, LDD>=, ORD<, ORD<=, ORD<>, ORD=, ORD>, ORD>=
BCD conversions	BCD, BCDP, DBCD, DBCDP
BIN conversions	BIN, BINP, DBIN, DBINP
16-bit data transfer	MOV, MOVP
16-bit data negation transfer	CML, CMLP
32-bit data transfer	DMOV, DMOVP
32-bit data negation transfer	DCML, DCMLP
Floating decimal point data transfer(Single precision)	EMOV, EMOVP
Logical sum	DOR, DORP, WOR, WORP
Logical product	DAND, DANDP, WAND, WANDP
Exclusive OR	DXOR, DXORP, WXOR, WXORP
NON exclusive logical sum	DXNR, DXNRP, WXNR, WXNRP
BIN data increment	DDEC, DDECP, DEC, DECP, DINC, DINCP, INC, INCP
BIN → Floating point conversions(Single precision)	DFLT, DFLTP, FLT, FLTP
Floating point → BIN conversions(Single precision)	DINT, DINTP, INT, INTP

(1) Subset Processing

Subset processing is used to place limits on bit devices used by basic instructions and application instructions in order to increase processing speed.

Conditions which each device must meet for subset processing.

(a) When using word data

Device	Condition
Bit device	• Designates a bit device number in a factor of 16. • Only K4 can be designated for digit designation. • Does not perform indexing.
Word device	• Internal user device. • File register (R, ZR *1) • Multiple CPU shared device *1, *2 • Index register (Z) / Standard device register (Z) *1
Constants	• No limitations

(b) When using double word data

Device	Condition
Bit device	• Designates a bit device number in a factor of 16. • Only K8 can be designated for digit designation. • Does not perform indexing.
Word device	• Internal user device. • File register (R, ZR *1) • Multiple CPU shared device *1, *2 • Index register (Z) / Standard device register (Z) *1
Constants	• No limitations

(c) When using bit data

Device	Condition
Bit device	• Internal user device (indexing possible)
Word device	• Bit specification of internal user device • Bit specification of file register (R, ZR *1) • Bit specification of multiple CPU shared device *1, *2

*1: Only for Universal model QCPU

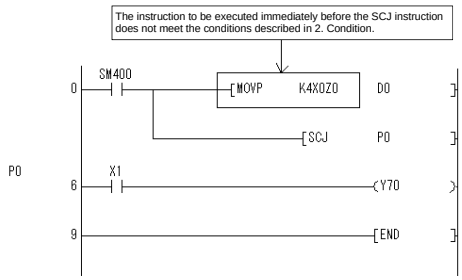
*2: Valid only for the multiple CPU high speed transmission area (from U3En\G10000)
(Excluding the case that indexing is executed for the head I/O number of the CPU module (U3En\G10000))

3. Program update method

(1) Insert the special relay (SM400) (or the NOP instruction) in immediately before the SCJ instruction as shown in the following program.

<Before updating>

[Ladder Mode]

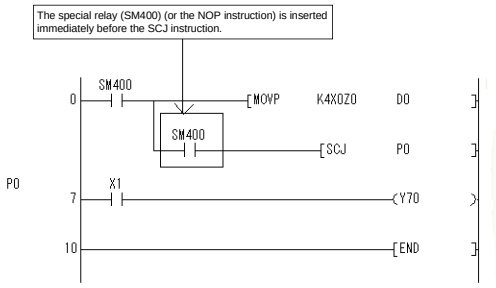


[List Mode]

Step	Instruction	Device
0	LD	SM400
1	MOVP	K4X0Z0 D0
4	SCJ	P0
6	P0	
7	LD	X1
8	OUT	Y70
9	END	
10		

<After updating>

[Ladder Mode]

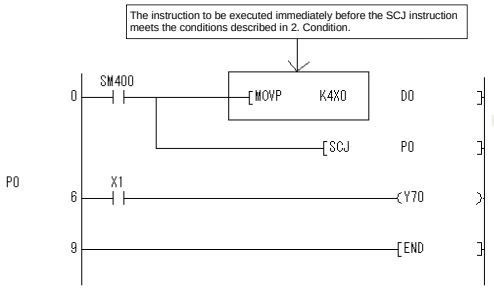


[List Mode]

Step	Instruction	Device
0	LD	SM400
1	MOVP	K4X0Z0 D0
4	AND	SM400
5	SCJ	P0
7	P0	
8	LD	X1
9	OUT	Y70
10	END	
11		

(2) If the immediately preceding instruction meets the conditions described in 2.Condition above, inserting the special relay SM400 (or NOP instruction) is not required. Therefore, use the existing program as shown below.

[Ladder Mode]



[List Mode]

Step	Instruction	Device
0	LD	SM400
1	MOVP	K4X0 D0
4	SCJ	P0
6	P0	
7	LD	X1
8	OUT	Y70
9	END	
10		