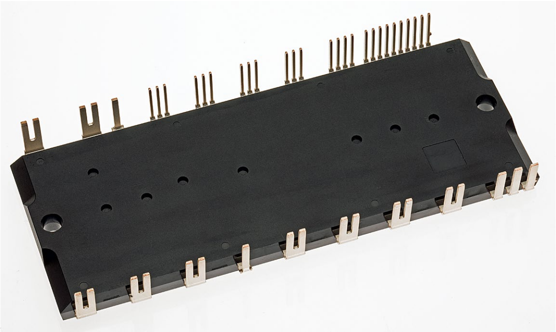
< DIPIPM >

PSS75NE1CT

TRANSFER MOLDING TYPE
INSULATED TYPE

OUTLINE



MAIN FUNCTION

CI (Converter + Inverter) type IPM

- 3-phase Inverter
- 3-phase Converter

RATING

- Inverter part : 75A/1200V (CSTBT)

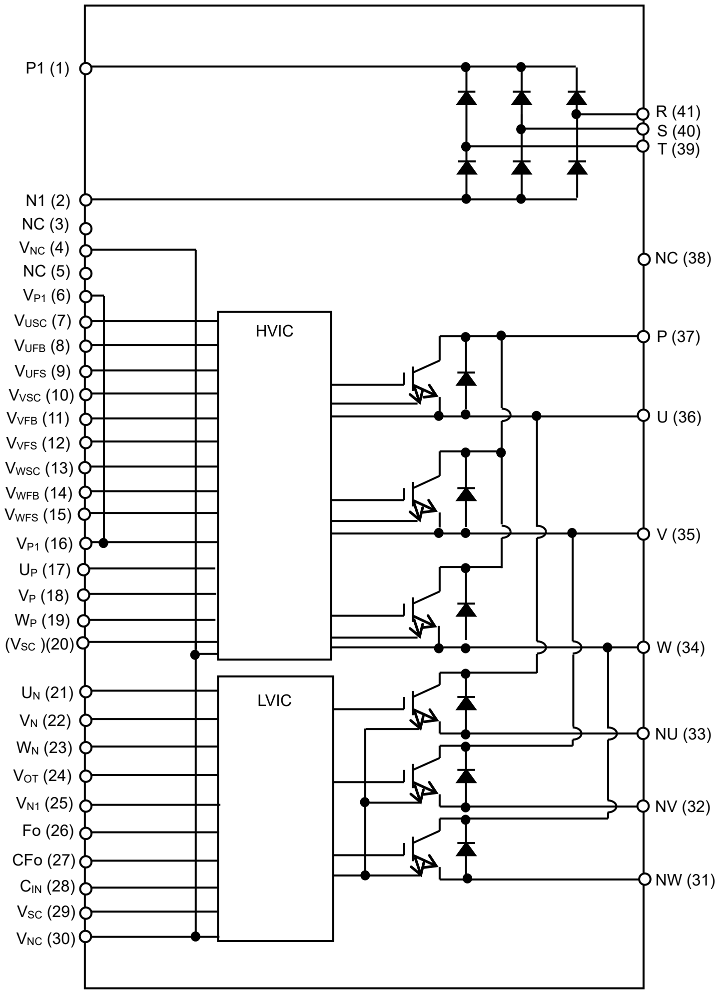
APPLICATION

- AC400V three phase motor inverter drive

INTEGRATED DRIVE, PROTECTION AND SYSTEM CONTROL FUNCTIONS

- For P-side : Drive circuit, High voltage high-speed level shifting, Control supply under-voltage (UV) protection
- For N-side : Drive circuit, Control supply under-voltage protection (UV), Short circuit protection (SC)
- Fault signaling : Corresponding to SC fault (N-side IGBT), UV fault (N-side supply)
- Temperature output : Outputting LVIC temperature by analog signal
- Input interface : 3.3, 5V line (High Active)
- UL Recognized : UL1557 File E323585

INTERNAL CIRCUIT



*It is necessary to short the V_{USC}-V_{UFS}, V_{VSC}-V_{VFS}, V_{WSC}-V_{WFS} pins.

MAXIMUM RATINGS (T_j = 25°C, unless otherwise noted)

INVERTER PART

Symbol	Parameter	Condition	Ratings	Unit
V_{CC}	Supply voltage	Applied between P-NU, NV, NW	800	V
$V_{CC(surge)}$	Supply voltage (surge)	Applied between P-NU, NV, NW	1000	V
V_{CES}	Collector-emitter voltage		1200	V
$\pm I_C$	Each IGBT collector current	T_C= 25°C (Note 1)	75	A
$\pm I_{CP}$	Each IGBT collector current (peak)	T_C= 25°C, up to 1ms	112.5	A
T_{jop}	Junction temperature	Continuous operation (Note 2)	-30~+150	°C
T_{jmax}	Maximum Junction temperature	Instantaneous event(overload)	175	°C

Note1: Pulse width and period are limited due to junction temperature.
Note2: The maximum junction temperature rating is 175°C. But for safe operation, it is recommended to limit the average junction temperature up to 150°C.

CONVERTER PART

Symbol	Parameter	Condition	Ratings	Unit
V_{RRM}	Repetitive peak reverse voltage		1600	V
I_O	DC output current	3φ rectifying circuit	75	A
I_{FSM}	Surge forward current	Half sine at 60Hz, Peak value, Non-repetitive	600	A
I^2t	I^2t for fusing	Value for 1 cycle of surge current	1440	A^2s
T_j	Junction temperature	(Note 3)	-30~+150	°C

Note3: The maximum junction temperature rating is 150°C. But for safe operation, it is recommended to limit the average junction temperature up to 125°C.

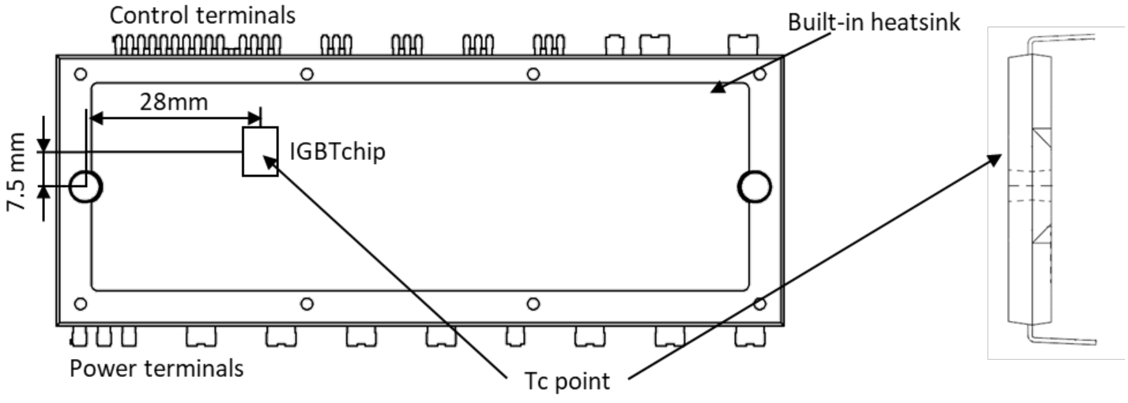
CONTROL (PROTECTION) PART

Symbol	Parameter	Condition	Ratings	Unit
V_D	Control supply voltage	Applied between V_{P1}-V_{PC}, V_{N1}-V_{NC}	20	V
V_{DB}	Control supply voltage	Applied between V_{UFB}-V_{UFS}, V_{VFB}-V_{VFS}, V_{WFB}-V_{WFS}	20	V
V_{IN}	Input voltage	Applied between U_P, V_P, W_P-V_{PC}, U_N, V_N, W_N-V_{NC}	-0.5~V_D+0.5	V
V_{FO}	Fault output supply voltage	Applied between F_O-V_{NC}	-0.5~V_D+0.5	V
I_{FO}	Fault output current	Sink current at F_O terminal	5	mA
V_{SC}	Current sensing input voltage	Applied between CIN-V_{NC}	-0.5~V_D+0.5	V

TOTAL SYSTEM

Symbol	Parameter	Condition	Ratings	Unit
$V_{CC(PROT)}$	Self protection supply voltage limit (Short circuit protection capability)	V_D = 13.5~16.5V, Inverter Part T_j = 150°C, non-repetitive, up to 2μs	800	V
T_C	Module case operation temperature	Tc measurement point is defined in Fig.1.	-30~+125	°C
T_{stg}	Storage temperature		-40~+125	°C
V_{iso}	Isolation voltage	60Hz, Sinusoidal, AC 1min, between connected all pins and heat sink plate	2500	V_{rms}

Fig. 1: T_C MEASUREMENT POINT



THERMAL RESISTANCE

Symbol	Parameter	Condition	Limits Min.	Limits Typ.	Limits Max.	Unit
$R_{th(j-c)Q}$	Junction to case thermal resistance (Note 4)	Inverter IGBT part (per 1/6 module)	-	-	0.50	K/W
$R_{th(j-c)F}$		Inverter FWDi part (per 1/6 module)	-	-	0.95	K/W
$R_{th(j-c)R}$		Converter part (per 1/6module)			0.90	K/W

Note 4: Grease with good thermal conductivity and long-term endurance should be applied evenly with about +100μm~+200μm on the contacting surface of DIPIPM and heat-sink. The contacting thermal resistance between DIPIPM case and heat sink Rth(c-f) is determined by the thickness and the thermal conductivity of the applied grease. For reference, Rth(c-f) (per 1chip) is about 0.25K/W when the grease thickness is 20μm and the thermal conductivity is 1.0W/m·K

ELECTRICAL CHARACTERISTICS (T_j = 25°C, unless otherwise noted)

INVERTER PART

Symbol	Parameter	Condition		Limits Min.	Limits Typ.	Limits Max.	Unit
$V_{CE(sat)}$	Collector-emitter saturation voltage	V_D=V_{DB}=15V, V_{IN}=5V, I_C= 75A	T_j= 25°C	-	1.50	1.90	V
			T_j= 125°C	-	1.80	2.30	
V_{EC}	FWDi forward voltage	V_{IN}= 0V, -I_C= 75A		-	1.85	2.40	V
t_{on}	Switching times	V_{CC}= 600V, V_D= V_{DB}= 15V I_C= 75A, T_j= 125°C, V_{IN}= 0↔5V Inductive Load (upper-lower arm)		1.40	2.30	3.30	μs
$t_{C(on)}$				-	0.40	0.85	μs
t_{off}				-	2.70	3.80	μs
$t_{C(off)}$				-	0.30	0.95	μs
t_{rr}				-	0.30	-	μs
I_{CES}	Collector-emitter cut-off current	V_{CE}=V_{CES}		-	-	1	mA

CONVERTER PART

Symbol	Parameter	Condition	Limits Min.	Limits Typ.	Limits Max.	Unit
I_{RRM}	Repetitive reverse current	V_R=V_{RRM}	-	-	0.5	mA
V_F	Forward voltage drop	I_F=75A	-	1.30	1.75	V

CONTROL (PROTECTION) PART

Symbol	Parameter	Condition		Limits Min.	Limits Typ.	Limits Max.	Unit
I_D	Circuit current	Total of V_{P1}-V_{PC}, V_{N1}-V_{NC}	V_D=15V, V_{IN}=0V	-	-	4.70	mA
			V_D=15V, V_{IN}=5V	-	-	4.70	
I_{DB}		Each part of V_{UFB}-V_{UFS}, V_{VFB}-V_{VFS}, V_{WFB}-V_{WFS}	V_{DB}=15V, V_{IN}=0V	-	-	2.40	
			V_{DB}=15V, V_{IN}=5V	-	-	2.40	
I_{SC}	Short circuit trip level	Rs=30.1Ω (±1%), Not connecting outer shunt resistors to NU,NV,NW terminals (Note 5)		112.5	-	-	A
UV_{DBt}	P-side Control supply under-voltage protection(UV)		Trip level	10.0	-	12.3	V
UV_{DBr}			Reset level	10.4	-	12.9	V
UV_{Dt}	N-side Control supply under-voltage protection(UV)		Trip level	10.3	-	12.5	V
UV_{Dr}			Reset level	10.8	-	13.0	V
V_{FOH}	Fault output voltage	V_{SC} = 0V, F_O terminal pulled up to 5V by 10kΩ		4.9	-	-	V
V_{FOL}		V_{SC} = 1V, I_{FO} = 1mA		-	-	0.95	V
t_{FO}	Fault output pulse width	C_{FO}=22nF (Note 6)		1.6	2.4	-	ms
I_{IN}	Input current	V_{IN} = 5V		0.7	1.0	1.5	mA
$V_{th(on)}$	ON threshold voltage	Applied between U_P, V_P, W_P-V_{NC}, U_N, V_N, W_N-V_{NC}		-	-	2.6	V
$V_{th(off)}$	OFF threshold voltage			0.8	-	-	V
V_{OT}	Temperature output	LVIC temperature=100°C, pull-down resistor=5.1kΩ (Note 7)		2.89	3.02	3.14	V

Note 5: Short circuit protection detects sense current divided from main current at N-side IGBT only. In the case that outer shunt resistor is inserted into main current path, protection current level Isc changes. For over -current protection by outside circuit, set the protection level under I_{CP}.
6: Fault signal is output when short circuit or N-side control supply under-voltage protection works. The fault output pulse-width t_{FO} depends on the capacitance of C_{FO}. (C_{FO} (typ.) = t_{FO} x 9.1 x 10^{-6}) [F])
7: DIPIPM doesn't shut down IGBTs and output fault signal automatically when temperature rises excessively. When temperature exceeds the protective level that user defined, controller (MCU) should stop immediately. Temperature of LVIC vs. V_{OT} output characteristics is described in Fig.2. These minimum and maximum curves are based on theoretical designed value excluding LVIC temperature=100°C limits.

Fig. 2 Temperature of LVIC vs. V_{OT} Output Characteristics
(These minimum and maximum curves are based on theoretical designed value excluding LVIC temperature=100°C limits.)

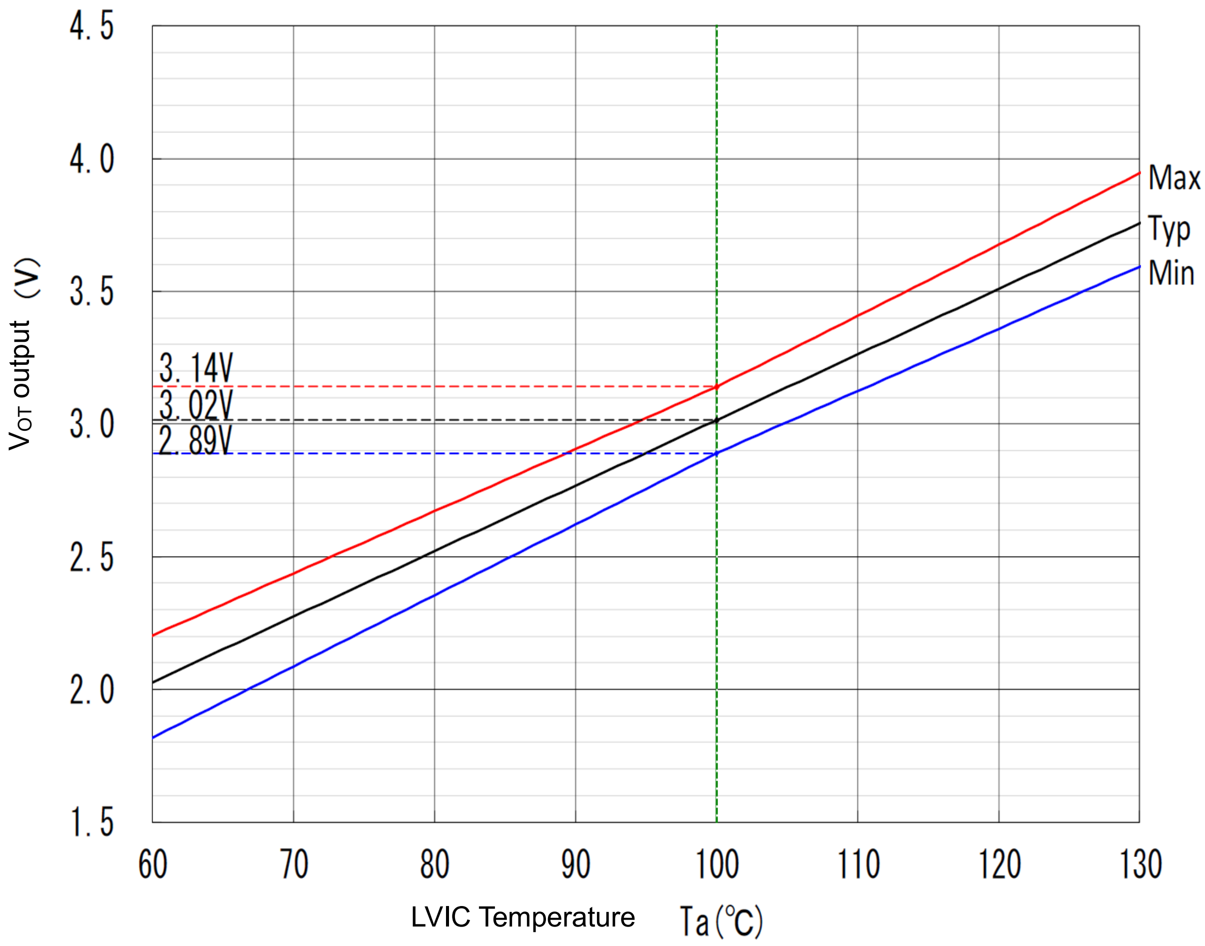
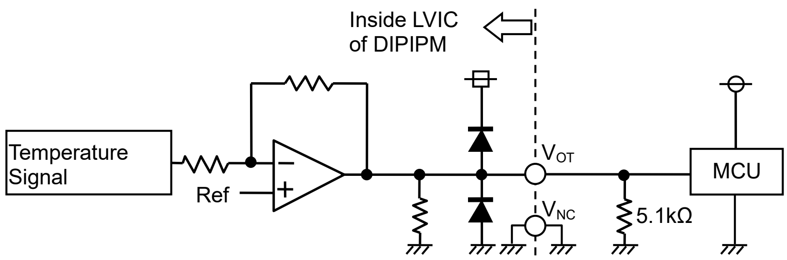


Fig. 3 V_{OT} output circuit



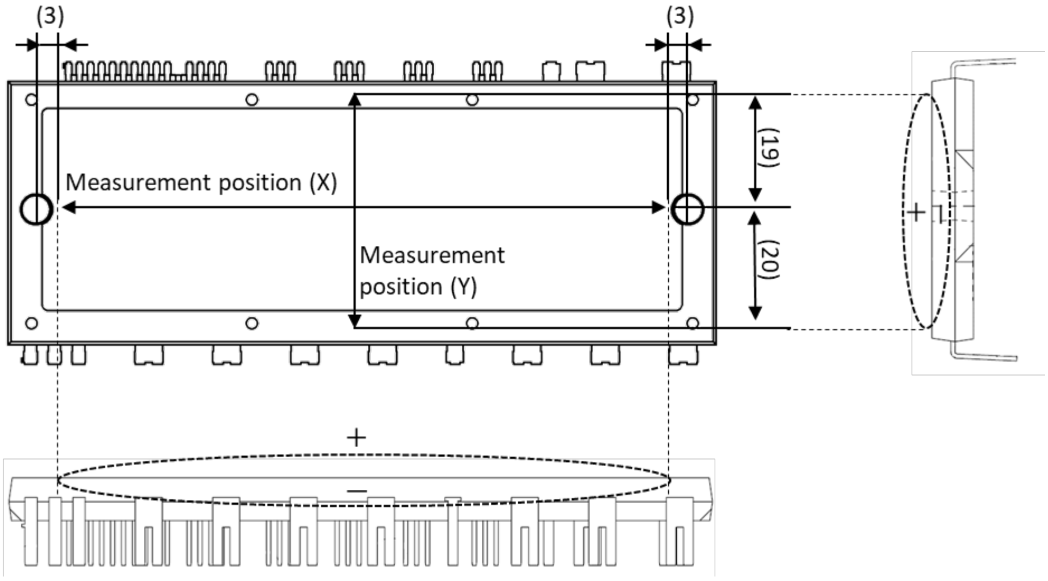
(1) It is recommended to insert 5.1kΩ pull down resistor for getting linear output characteristics at low temperature (below room temperature). When the pull down resistor is inserted between V_{OT} and V_{NC} (control GND), the extra circuit current, which is calculated approximately by V_{OT} output voltage divided by pull down resistance, flows as LVIC circuit current continuously. In the case of using V_{OT} for detecting only higher temperature than room temperature, it isn't necessary to insert the pull down resistor.
(2) In the case of using V_{OT} with low voltage controller like 3.3V MCU, V_{OT} output might exceed control supply voltage 3.3V when temperature rises excessively. If system uses low voltage controller, it is recommended to insert a clamp Di between control supply of the controller and V_{OT} output for preventing over voltage destruction.
(3) In the case of not using V_{OT}, leave V_{OT} output NC (No Connection).

Refer the application note for this product about the usage of V_{OT}.

MECHANICAL CHARACTERISTICS AND RATINGS

Parameter	Condition	Reference	Limits Min.	Limits Typ.	Limits Max.	Unit
Mounting torque	Mounting screw : M4 (Note 8)	JEITA-ED-4701 402 method Ⅱ	0.98	1.18	1.47	N·m
Terminal strength pulling	Weight power terminal:40N control terminal:10N	JEITA-ED-4701 401 method Ⅰ	10	-	-	s
Terminal strength bending	Load 10N, 90deg. bend	JEITA-ED-4701 401 method Ⅲ	2	-	-	times
Weight			-	89	-	g
Heat radiation part flatness	(Note 9)		-50	-	130	μm

Note 8: Plain washers (ISO 7089~7094) are recommended.
Note 9: Measurement point of heat-sink flatness



(Unit: mm)

RECOMMENDED OPERATION CONDITIONS

Symbol	Parameter	Condition	Limits Min.	Limits Typ.	Limits Max.	Unit
V_{CC}	Supply voltage	Applied between P-NU, NV, NW	300	600	800	V
V_D	Control supply voltage	Applied between V_{P1}-V_{NC}, V_{N1}-V_{NC}	13.5	15.0	16.5	V
V_{DB}	Control supply voltage	Applied between V_{UFB}-V_{UFS}, V_{VFB}-V_{VFS}, V_{WFB}-V_{WFS}	13.0	15.0	18.5	V
ΔV_D, ΔV_{DB}	Control supply variation		-1	-	+1	V/μs
t_{dead}	Arm shoot-through blocking time	For each input signal	2.5	-	-	μs
f_{PWM}	PWM input frequency	$T_C \leq 125°C$, $T_j \leq 150°C$	-	-	20	kHz
V_{NC}	V_{NC} terminal voltage	Between V_{NC}-NU, NV, NW (including surge)	-5.0	-	+5.0	V
PWIN(on)	Minimum input pulse width	(Note 10)	3.0	-	-	μs
PWIN(off)	Minimum input pulse width	(Note 11)	3.0	-	-	μs

Note 10: DIPIPM might not make response if the input signal pulse width is less than PWIN(on).
Note 11: DIPIPM might make no response or delayed response (P-side IGBT only) for input pulse width less than PWIN(off). Over rated collector current (Ic) operation, DIPIPM might make delayed response even if the input signal pulse width is PWIN(off) or more. The timing charts are described as below.

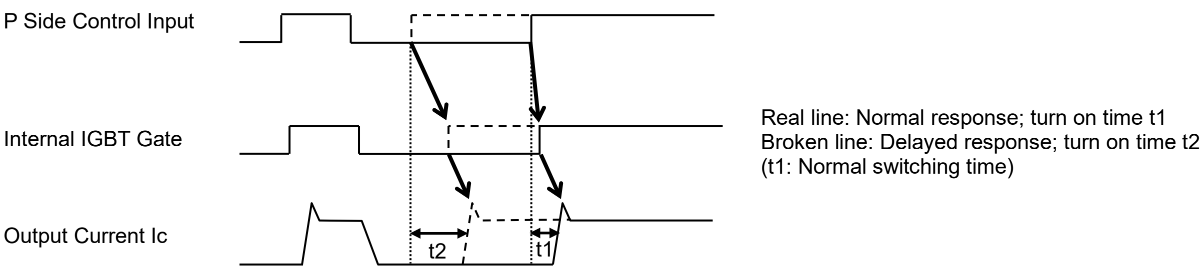
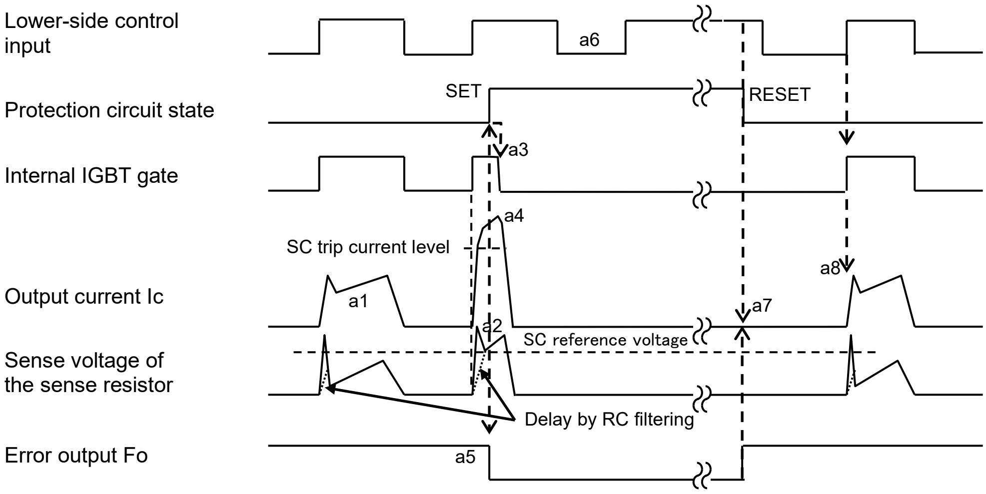


Fig. 4 Timing Charts of DIPIPM Protective Functions

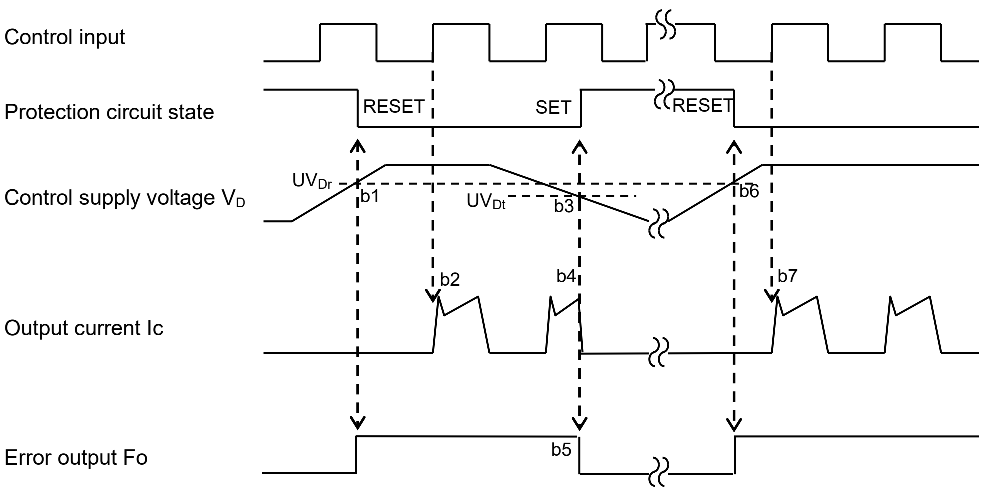
[A] Short-Circuit Protection (N-side only with the external sense resistor and RC filter)

a1. Normal operation: IGBT ON and outputs current.
a2. Short circuit current detection (SC trigger)
(It is recommended to set RC time constant 1.5~2.0μs so that IGBT shut down within 2.0μs when SC occurs.)
a3. All N-side IGBT's gates are hard interrupted.
a4. All N-side IGBTs turn OFF.
a5. F_O outputs with a fixed pulse width determined by the external capacitor C_{FO}.
a6. Input = “L”: IGBT OFF
a7. Fo finishes output, but IGBTs don't turn on until inputting next ON signal (L→H).
(IGBT of each phase can return to normal state by inputting ON signal to each phase.)
a8. Normal operation: IGBT ON and outputs current.



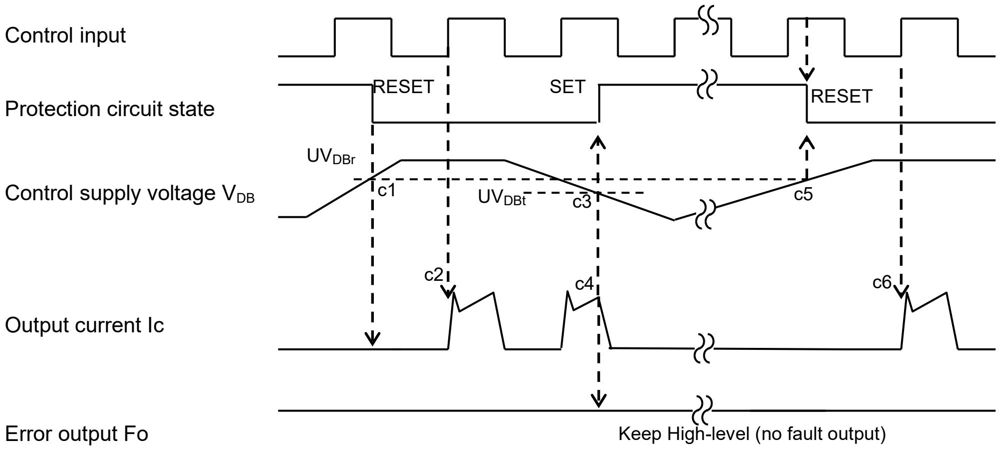
[B] Under-Voltage Protection (N-side, UV_D)

b1. Control supply voltage V_D exceeds under voltage reset level (UV_{Dr}), but IGBT turns ON by next ON signal (L→H).
(IGBT of each phase can return to normal state by inputting ON signal to each phase.)
b2. Normal operation: IGBT ON and outputs current.
b3. V_D level drops to under voltage trip level. (UV_{Dt}).
b4. All N-side IGBTs turn OFF in spite of control input condition.
b5. Fo outputs for the period determined by the capacitance C_{FO}, but output is extended during V_D keeps below UV_{Dr}.
b6. V_D level reaches UV_{Dr}.
b7. Normal operation: IGBT ON and outputs current by next ON signal (L→H).



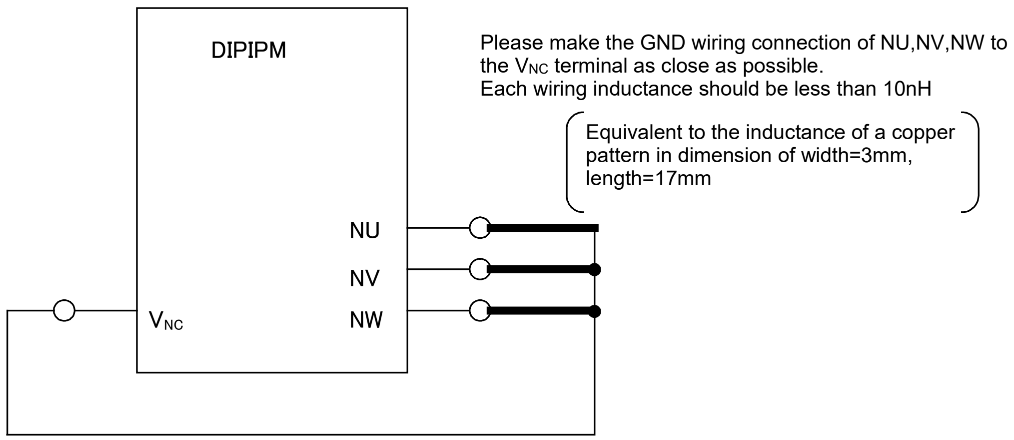
[C] Under-Voltage Protection (P-side, UV_{DB})

c1. Control supply voltage V_{DB} rises. After the voltage reaches under voltage reset level UV_{DBr}, IGBT turns on by next ON signal (L→H).
c2. Normal operation: IGBT ON and outputs current.
c3. V_{DB} level drops to under voltage trip level (UV_{DBt}).
c4. IGBT of corresponding phase only turns OFF in spite of control input signal level, but there is no F_O signal output.
c5. V_{DB} level reaches UV_{DBr}.
c6. Normal operation: IGBT ON and outputs current by next ON signal (L→H).

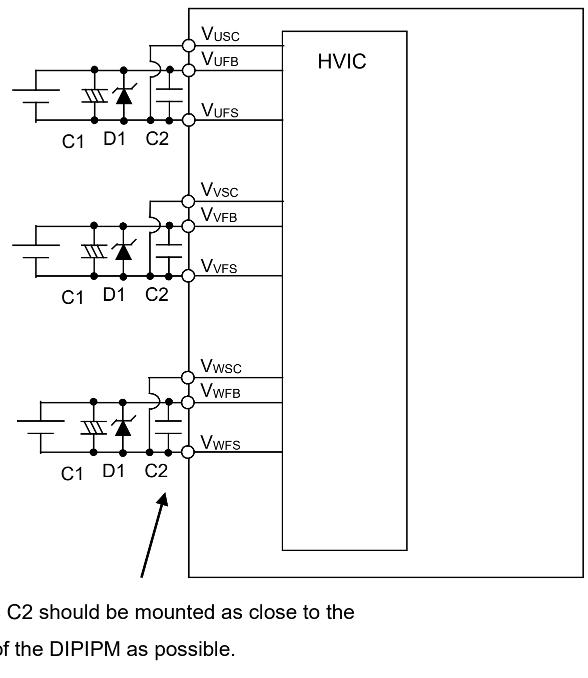


Peripheral circuits

1) Pattern Wiring Around N terminal

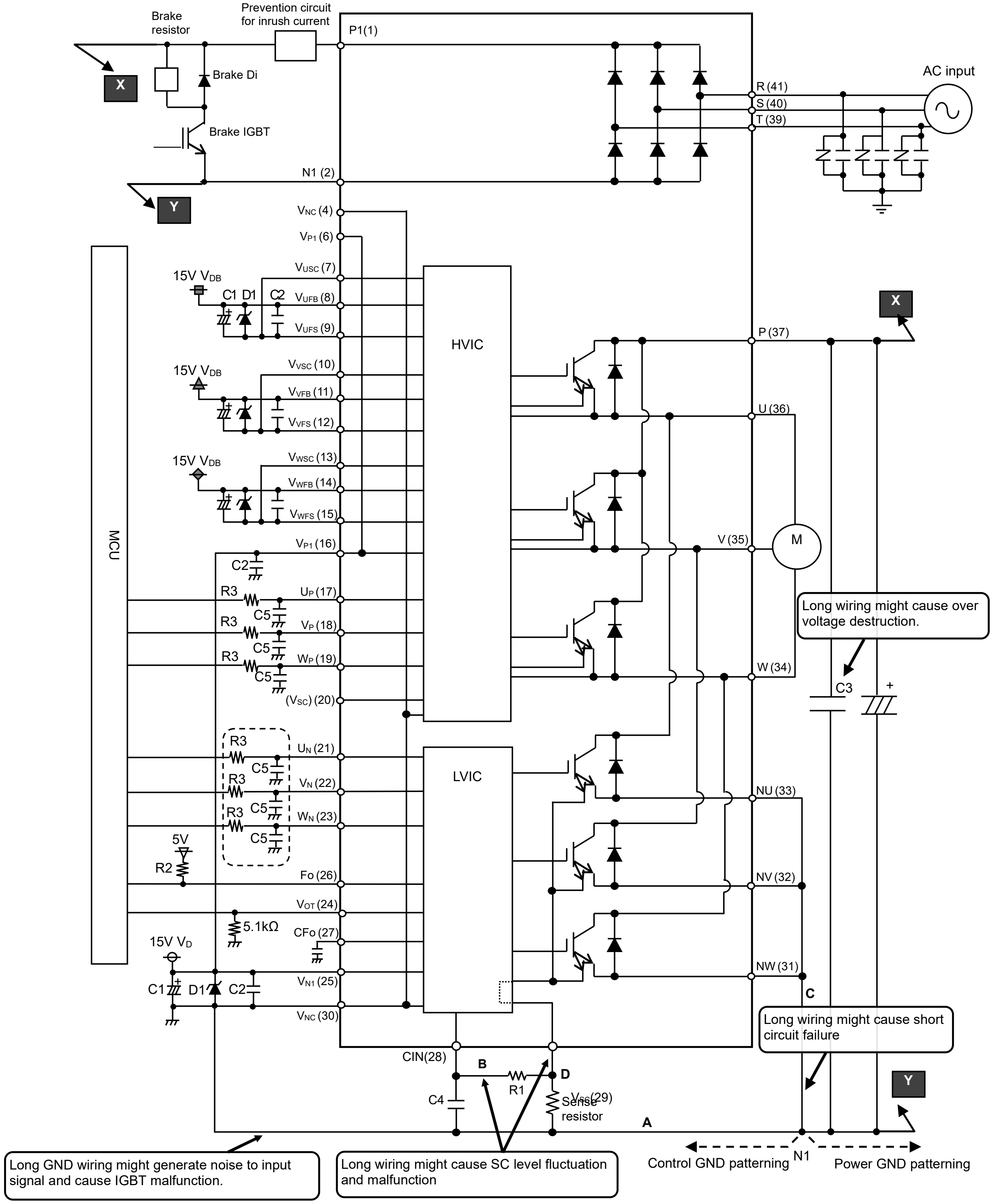


2) Circuit Around Control supply voltage V_{DB}



(1) All capacitors, especially C2 should be mounted as close to the terminals of the DIPIPM as possible. C1: good temperature, frequency characteristic electrolytic type, and C2: 0.1μ～2μF, good temperature, frequency and DC bias characteristic type should be used (SMD type is recommended).
(2) It is recommended to insert a Zener diode (24V,1W) between each pair of control supply terminals to prevent surge destruction.

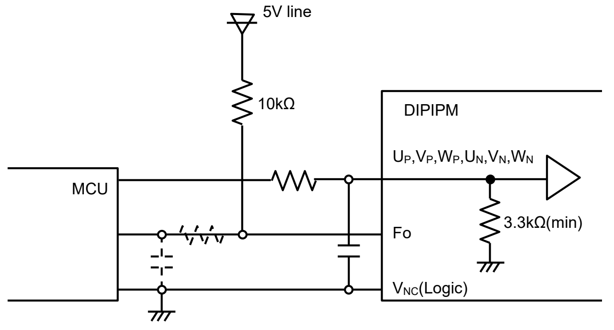
Fig. 5 Example of Application Circuit



Note for the previous application circuit

1 :If control GND and power GND are patterned by common wiring, it may cause malfunction by fluctuation of power GND level. It is recommended to connect control GND and power GND at only a N1 point at which NU, NV, NW are connected to power GND line.
2 :It is recommended to insert a Zener diode D1 (24V/1W) between each pair of control supply terminals to prevent surge destruction.
3 :To prevent surge destruction, the wiring between the smoothing capacitor and the P, N1 terminals should be as short as possible. Also, insert a snubber capacitor C3 of appropriate capacity (1μF or more) between the P-N1 terminals. Please design the capacity of the snubber capacitor so that it is optimized according to the wiring pattern etc..
4 :R1, C4 of RC filter for preventing protection circuit malfunction is recommended to select tight tolerance, temp-compensated type. The time constant R1C4 should be set so that SC current is shut down within 2μs. (1.5μs~2μs is general value.) SC interrupting time might vary with the wiring pattern, so the enough evaluation on the real system is recommended. If R1 is too small, it may lead to delay of protection. So R1 should be min. 10 times larger resistance than Rs. (100 times is recommended.)
5 :To prevent erroneous operation, the wiring of A, B, C should be as short as possible.
6 :For sense resistor, the variation within 1% (including temperature characteristics), low inductance type is recommended. And the over 0.03W is recommended, but it is necessary to evaluate in your real system finally.
7 :To prevent erroneous SC protection, the wiring from V_{SC} terminal to CIN filter should be divided at the point D that is close to the terminal of sense resistor. And the wiring should be patterned as short as possible.
8 :All capacitors should be mounted as close to the terminals of the DIPIPM as possible. (C1: good temperature, frequency characteristic electrolytic type, and C2: 0.1μ~2.0μF, good temperature, frequency and DC bias characteristic ceramic type are recommended.)
9 :Input drive is High-active type. There is a min. 3.3kΩ pull-down resistor in the input circuit of IC. To prevent malfunction, the wiring of each input should be as short as possible. And it is recommended to insert RC filter (e.g. R3=100Ω and C5=1000pF) and confirm the input signal level to meet the turn-on and turn-off threshold voltage. Thanks to HVIC inside the module, direct coupling to MCU without any opto-coupler or transformer isolation is possible.
10 :Fo output is open drain type. Fo output will be max 0.95V(@I_{FO}=1mA,25°C), so it should be pulled up to MCU or control power supply (e.g. 5V,15V) by a resistor that makes I_{Fo} up to 1mA. (In the case of pulled up to 5V, 10kΩ is recommended.)
11 :Error signal output width (t_{Fo}) can be set by the capacitor connected to C_{FO} terminal. C_{FO} (typ.) = t_{Fo} x 9.1 x 10^{-6} (F)
12 :If high frequency noise superimposed to the control supply line, IC malfunction might happen and cause erroneous operation. To avoid such problem, voltage ripple of control supply line should meet dV/dt ≤+/-1V/μs, Vripple≤2Vp-p.
13 :For DIPIPM, it isn't recommended to drive same load by parallel connection with other phase IGBT or other DIPIPM.
14 :No.4 and No.30 V_{NC} terminals (GND terminal for control supply) are connected mutually inside of DIPIPM+ and also No.6 and No.16 V_{P1} terminals are connected mutually inside, please connect either No.4 or No.30 terminal to GND and also connect either No.6 or No.16 terminal to supply and make the unused terminal leave no connection.
15 :Please connect the V_{USC}-V_{UFS}(7-9 terminal)、V_{VSC}-V_{VFS}(10-12 terminal)、V_{WSC}-V_{WFS}(13-15terminal) externally.
16 :Although 3, 5, 20 and 38 terminals are dummy terminals, it may have an electric potential, so make it a no connection.

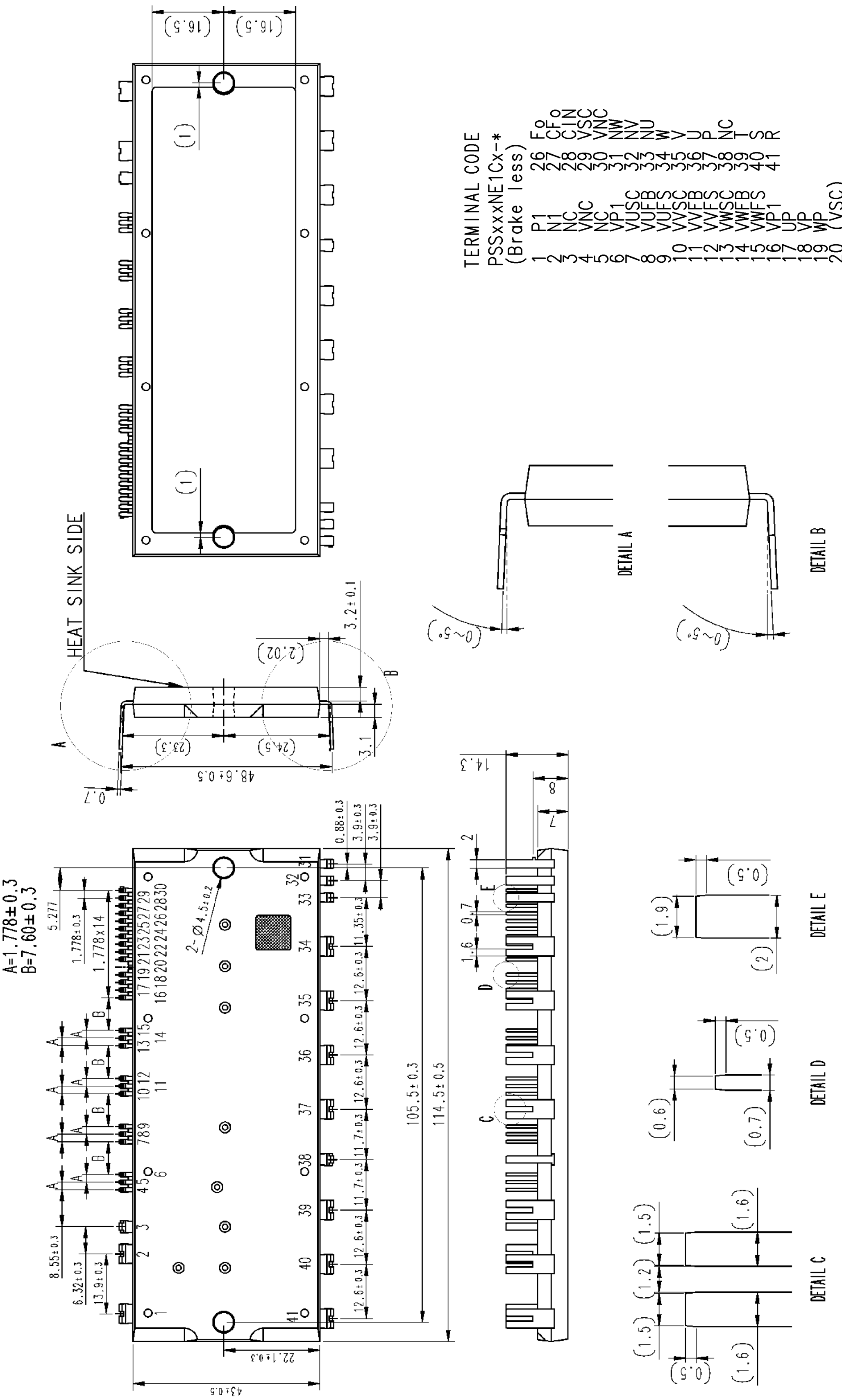
Fig. 6 MCU I/O Interface Circuit



Note)
Design for input RC filter depends on the PWM control scheme used in the application and the wiring impedance of the printed circuit board.
The DIPIPM input signal interface integrates a min. 3.3kΩ pull-down resistor. Therefore, when using RC filter, be careful to satisfy turn-on threshold voltage requirement.
Fo output is open drain type. It should be pulled up to the positive side of 5V or 15V power supply with the resistor that limits Fo sink current I_{Fo} under 1mA. In the case of pulling up to 5V supply, over 5.1kΩ is needed. (10kΩ is recommended.)

Fig. 7 Package Outlines

Dimensions in mm



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